# Intel® Stratix® 10

## INTEL® STRATIX® 10 DX PRODUCT TABLE

| | PRODUCT LINE | DX 1100 | DX 2100 | DX 2800 |
|---|---|---|---|---|
| Resources | Logic elements (LEs)[1] | 1,325,000 | 2,073,000 | 2,753,000 |
| | Adaptive logic modules (ALMs) | 449,280 | 702,720 | 933,120 |
| | ALM registers | 1,797,120 | 2,810,880 | 3,732,480 |
| | Hyper-Registers from Intel® Hyperflex™ FPGA architecture | Millions of Hyper-Registers distributed throughout the monolithic FPGA fabric | | |
| | Programmable clock trees synthesizable | Hundreds of synthesizable clock trees | | |
| | HBM2 High-bandwidth DRAM memory stacks | – | 2 | – |
| | HBM2 High-bandwidth DRAM memory size (GB) | – | 8 | – |
| | eSRAM memory blocks | – | 2 | – |
| | eSRAM memory size (Mb) | – | 94.5 | – |
| | M20K memory blocks | 5,461 | 6,847 | 11,721 |
| | M20K memory size (Mb) | 107 | 134 | 229 |
| | MLAB memory size (Mb) | 7 | 11 | 15 |
| | Variable-precision digital signal processing (DSP) blocks | 2,592 | 3,960 | 5,760 |
| | 18 x 19 multipliers | 5,184 | 7,920 | 11,520 |
| | Peak fixed-point performance (TMACS)[2] | 10.4 | 15.8 | 23.0 |
| | Peak floating-point performance (TFLOPS)[3] | 4.1 | 6.3 | 9.2 |
| I/O and Architectural Features | Secure device manager | AES-256/SHA-256 bitstream encryption/authentication, physically unclonable function (PUF), ECDSA 256/384 boot code authentication, side channel attack protection | | |
| | Hard processor system[4] | Quad-core 64-bit Arm* Cortex*-A53 up to 1.5 GHz with 32KB I/D cache, NEON* coprocessor, 1 MB L2 cache, direct memory access (DMA), system memory management unit, cache coherency unit, hard memory controllers, USB 2.0 x2, 1G EMAC x3, UART x2, SPI x4, I2C x5, general purpose timers x7, watchdog timer x4 | | |
| | | Yes | – | – |
| | Maximum user I/O pins | 528 | 612 | 816 |
| | Maximum LVDS pairs 1.6 Gbps (RX or TX) | 264 | 306 | 408 |
| | Total full duplex transceiver count - non return to zero (NRZ) | 32 | 84 | 84 |
| | GXE transceiver count - PAM4 (up to 57.8 Gbps) or NRZ (up to 28.9 Gbps) | 8 PAM-4, or 16 NRZ | 12 PAM-4, or 24 NRZ | 4 PAM-4, or 8 NRZ |
| | GXP transceiver count - NRZ (up to 16 Gbps) | 16 | 60 | 76 |
| | UPI/PCI Express* (PCIe*) Gen4 x16 hard intellectual property (IP) blocks (configurable for UPI or PCIe operation) | - | 3 | 3 |
| | PCI Express Gen4 x16 hard IP blocks (supports PCIe only) | 1 | - | 1 |
| | 100G Ethernet media access control (MAC) + forward error correction (FEC) hard IP blocks | 4 | 4 | 2 |
| | Memory devices supported | DDR4, DDR3, DDR2, DDR, QDR II, QDR II+, RLDRAM II, RLDRAM 3 | | |
| Package Options and I/O Pins: General-Purpose I/O (GPIO) Count, High-Voltage I/O Count, LVDS Pairs, P-Tile Transceiver Count and E-Tile Transceiver Count | | | | |
| F1760 pin (42.5 mm x 42.5 mm, 1.0 mm pitch) | | 528,0,264,16,16 | – | – |
| F2597 pin (52.5 mm x 52.5 mm, 1.0 mm pitch) | | – | 612,0,306,60,24 | – |
| F2912 pin (55 mm x 55 mm, 1.0 mm pitch) | | – | – | 816,0,408,76,8 |

Notes:
1. LE counts valid in comparing across Intel FPGA devices, and are conservative vs. competing FPGAs.
2. Fixed-point performance assumes the use of pre-adder.
3. Floating-point performance is IEEE-754 compliant single-precision.
4. Quad-core Arm Cortex-A53 hard processor system present in select Intel Stratix 10 DX devices.
5. All data is preliminary and subject to change without prior notice.

816,0,408,76,8 Numbers indicate total GPIO count, high-voltage I/O count, LVDS pairs, P-Tile transceiver count, E-Tile transceiver count.

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| PRODUCT LINE | DX 1100 |
|---|---|
| Processor | Quad-core 64 bit Arm Cortex-A53 MPCore* processor |
| Maximum processor frequency | 1.5 GHz[1] |
| Processor cache and co-processors | • L1 instruction cache (32 KB)<br>• L1 data cache (32 KB) with error correction code (ECC)<br>• Level 2 cache (1 MB) with ECC<br>• Floating-point unit (FPU) single and double precision<br>• Arm NEON media engine<br>• Arm CoreSight* debug and trace technology<br>• System Memory Management Unit (SMMU)<br>• Cache Coherency Unit (CCU) |
| Scratch pad RAM | 256 KB |
| HPS DDR memory | DDR4, DDR3 (Up to 64 bit with ECC) |
| Direct memory access (DMA) controller | 8 channels |
| EMAC | 3X 10/100/1000 Ethernet media access controller (EMAC) with integrated DMA |
| USB on-the-go (OTG) controller | 2X USB OTG with integrated DMA |
| UART controller | 2X UART 16550 compatible |
| Serial peripheral interface (SPI) controller | 4X SPI |
| $I^2C$ controller | 5X $I^2C$ |
| Quad SPI flash controller | 1X SIO, DIO, QIO SPI flash supported |
| SD/SDIO/MMC controller | 1X eMMC 4.5 with DMA and CE-ATA support |
| NAND flash controller | • 1X ONFI 1.0 or later<br>• 8 and 16 bit support |
| General-purpose timers | 4X |
| Software-programmable general-purpose I/Os (GPIOs) | Maximum 48 GPIOs |
| HPS DDR Shared I/O | 3X 48 - May be assigned to HPS for HPS DDR access |
| Direct I/Os | 48 I/Os to connect HPS peripherals directly to I/O |
| Watchdog timers | 4X |
| Security | Secure device manager, Advanced Encryption Standard (AES) AES-256/SHA-256 bitsream encryption/authentication, PUF, ECDSA 256/384 boot code authentication, side channel attack protection |

Notes:
1. With overdrive feature.