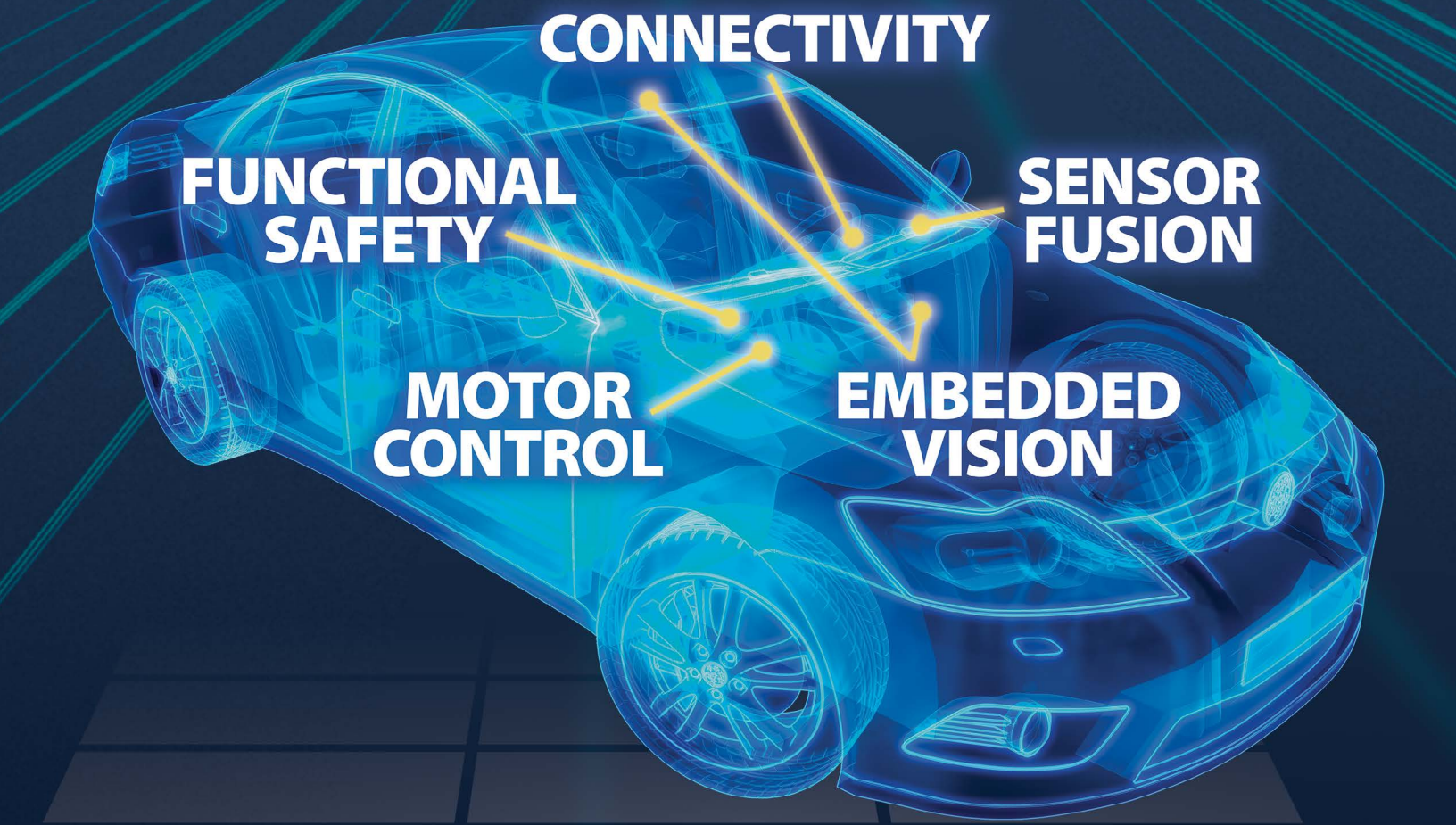
Q1 2017

AUTOMOTIVE

Paving the way to productivity



FPGAs | DESIGN TOOLS | IP

SoCs | AUTOSAR | POWER MANAGEMENT

For more than twelve years, Altera has been delivering AEC-Q100 qualified programmable logic devices (PLD), including MAX® CPLDs, Cyclone®, and MAX 10 family of FPGAs and SoCs, to our valued automotive OEM and Tier 1 customers. We understand the rigorous quality, reliability, and supply-chain requirements of our automotive customers and have implemented several programs to address these requirements, such as zero defect philosophy, continuous improvement, and product lifecycles of more than 15 years.

WHY FPGA?

Market research indicates FPGAs and PLDs in automotive will grow at double digit compound annual growth rates (CAGR) over the next several years. Altera's key automotive focus areas include some of the fastest growing segments in the industry, such as Infotainment and Driver Information, Advanced Driver Assistance System (ADAS), and E-Vehicle and Powertrain. Each of these application areas are undergoing a metamorphosis sparked by the proliferation of electronic content in vehicles and the associated megatrends driving them. Why the need for programmable logic in automotive? Three reasons: Scalability, flexibility, and raw performance. FPGAs are the only solution that are able to truly scale architectures from entry-level to luxury model vehicles by offering a wide range of logic densities, optional embedded ARM® cores and peripherals, and a single software development flow. This helps engineering managers and system designers get their products to market faster, more efficiently, and at a lower total cost of ownership, while maintaining the ability to make last minute tweaks prior to production launch.

SAFETY FIRST

Functional safety has long been a key strategic imperative for us, and Altera was the first FPGA supplier to achieve IEC 61508 functional safety certification[1] for the industrial market. That early commitment and investment has put us in a leading position to execute on our ISO 26262 functional safety plan for automotive applications. The Cyclone V SoC safety manual (automotive functional safety data pack) and device level FMEDA are available now, and the full qualification to ISO 26262 is expected by mid-2015. Altera is an active member of the ISO 26262 working group and our functional safety manager co-chairs the ISO 19451 PLD sub-group, which helps to drive PLD requirements into the 2nd edition of the ISO 26262 standard.

GET TO MARKET FASTER

Altera's total solution offering helps our customers go from proof-of-concept to production in the shortest possible time. How? By complementing our silicon with best-in-class development tools to help software and hardware engineers port their designs to FPGA or create new ones from the ground up. We've got you covered whether it's industry standards like Open Computing Language (OpenCL™), AUTOSAR, Altera's own Quartus® II development tool, or complementary solutions such as DSP Builder that bridge between Quartus II software and MATLAB/Simulink. Many of our design tools and methodologies have been certified by TÜV Rheinland to ensure the highest level of quality, integrity, and safety. Lastly, every programmable logic device requires power management and Altera is the only FPGA supplier to offer optimized power management solutions. Altera's Enpirion® power management products deliver the industry's first family of PowerSoC DC-DC converters featuring integrated inductors. They provide an industry-leading combination of high-efficiency, small-footprint, and low-noise performance in an integrated product. Unlike discrete power products, these turnkey solutions give designers complete power systems that are fully simulated, characterized, and production qualified. With our new AEC-Q100 qualified Enpirion PowerSoCs, automotive system designers can now leverage both power management and programmable logic from a single trusted supplier. Altera is here to help you deliver a total proven solution on time.

[1] Certified by TÜV Rheinland

ADVANCED DRIVER ASSISTANCE SYSTEMS

Our FPGAs can help you keep pace with the rapid advancements in driver assistance technology and address the key challenges you face, including:

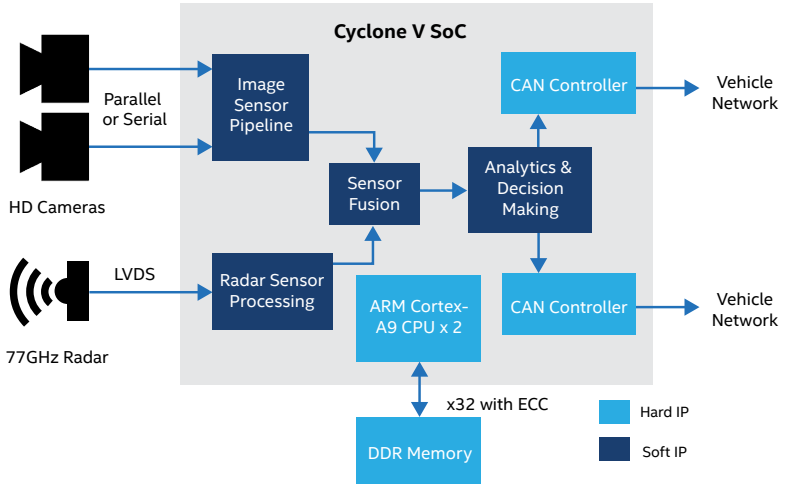
- Running multiple ADAS algorithms in parallel in a single low-cost SoC
- Delivering a scalable, low-cost solution tailored to address the requirements of different vehicle models
- Leveraging your intellectual property (IP) investments across multiple products
- Operating within the power and thermal limits of small camera modules without active cooling
- Incorporating new features to differentiate your products in the market

Our FPGAs provide an ideal platform for developing high-performance, low-power, low-cost ADAS systems with the optimal level of integration and flexibility. You can incorporate changes late in the design cycle and deploy in-field upgrades that let you differentiate your products and keep pace with your customers' expectations.

BENEFITS OF ALTERA FPGAS IN ADAS APPLICATIONS

- Parallel-processing architecture to run multiple ADAS algorithms simultaneously
- Scalability and differentiation, which allows you to include the latest features that can be deployed into all vehicle platforms
- Increased productivity using software-based design methodologies with open standards like OpenCL and model-based design using MATLAB and DSP Builder
- Simplified software development with an AUTOSAR-compliant MCAL layer developed using an ASIL-B methodology supported in our Cyclone V SoCs
- Ability to deliver the highest performance/watt vs. CPU, graphics processing unit (GPU), and ASSP devices
- Flexibility to be used as either the main processing device or a companion FPGA to offload high-performance processing tasks and incorporate new features

Forward Camera Sensor Fusion



FPGA Applications

- Forward, surround-view cameras
- 77-79 GHz digital radar
- V2X communications
- Radar and video sensor fusion

Cyclone V SoC Development Resources

- OpenCL-based design flow
- MATLAB to DSP Builder model-based design
- AUTOSAR v4.0.3 MCAL
- ISO 26262 functional safety data package

INFOTAINMENT

Automotive infotainment systems are an integral part of modern vehicle design and greatly influence global vehicle sales. You need to continually create compelling new technology that both rivals and complements the latest consumer devices while keeping up with the pace of product obsolescence common in consumer electronics.

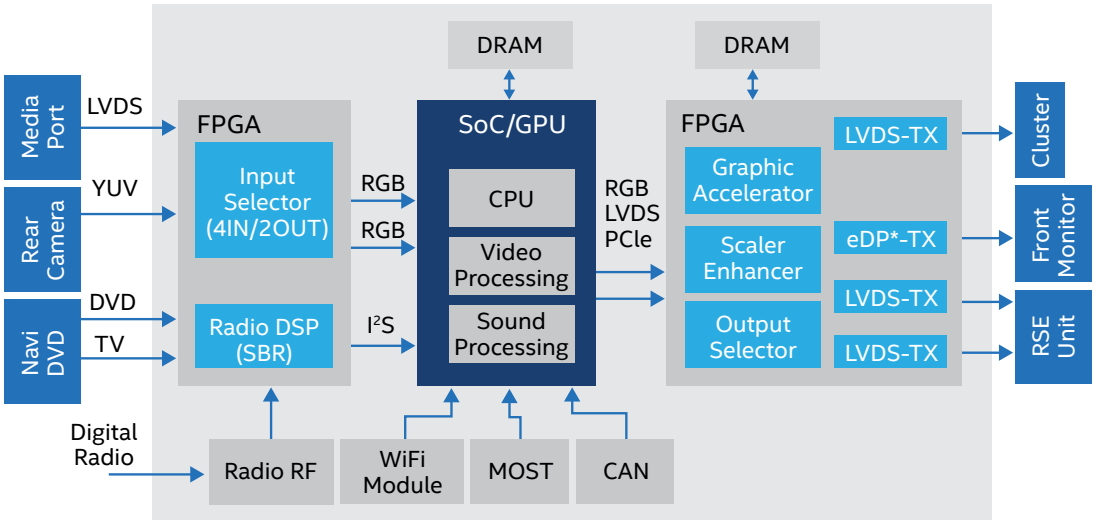
It is important to select the right main system processor to differentiate the system's user interface with the latest graphics. Should you choose a high-performance SoC with a GPU or a CPU with applications that can be upgraded with software? With multiple models to support, you may need to select several different SoCs due to system variations and emerging interfacing technologies. This is neither cost effective nor efficient usage of engineering resources.

By using our FPGAs as an I/O companion, you can support any combination of I/O interfaces. You may also leverage the FPGA as an efficient coprocessor to offload functions from your host main processor such as video scaling and graphics acceleration. With an FPGA, your system becomes easily scalable, enabling you to upgrade firmware on the fly to support multiple manufacturers, regions, and models with minimum changes to the hardware.

BENEFITS OF ALTERA FPGAS IN INFOTAINMENT APPLICATIONS

- Support multiple camera inputs in any bit rate or resolution via video select and front-end processing
- Support multiple display interfaces and offloads GPU
- Optimize system performance by integrating 2D/3D graphic accelerator, scalar, image enhancer, and interface protocol bridge
- Reduce cost by integrating radio digital signal processing (DSP) into FPGA with software-based radio IP
- Accelerate time to market by supporting the latest generation of interface standards in programmable logic
- Minimize PCB spins and future-proof your system with in-field upgrades to the FPGA

Pre and Post Video Processing Video Companion Application



* Embedded Display Port

ELECTRIC VEHICLES AND POWERTRAIN

The introduction of hybrid-electric vehicles (HEV) and electric vehicles (EV) have enabled breakthrough innovations and greater efficiency in electric motor controls, power conversion, and battery management systems.

The algorithms driving these systems require continuous upgrades and design changes to optimize performance. ASIC development cycles are too long to meet these market demands and microcontroller units (MCUs) are unable to keep up with performance requirements. Our FPGAs deliver hardware failsafe logic for insulated gate bipolar transistor (IGBT) bridge protection, efficient motor control with our model-based DSP Builder design flow, and hardware acceleration with faster control loops to improve energy efficiency, reduce noise, and improve reliability of electrical motors.

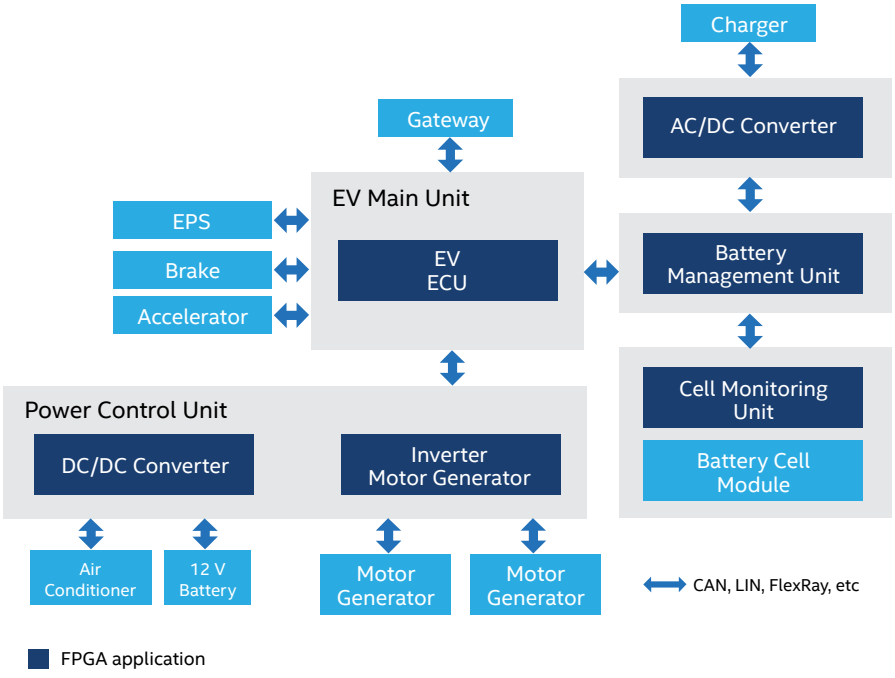
You can use FPGAs or CPLDs anywhere DSP is needed to improve system performance, such as the AC/DC converters, DC/DC converters, battery management systems, and motor inverter systems.

To accelerate your time to market and increase productivity, Altera and its partner network offer a variety of IP and tools. Our motor control IP includes pulse-width modulation (PWM), analog-to-digital (ADC) and digital encoder interfaces, and integrated customizable field-oriented control (FOC) reference designs.

BENEFITS OF ALTERA FPGAS IN HEV/EV APPLICATIONS

- Improve system performance by using hardware co-processor to accelerate your motor control algorithm
- Shorten design cycles with model-based design tools, safety methodology, and pre-qualified devices
- Designed for functional safety with IEC 61508-certified design tools, IP, and products (ISO 26262 certification expected mid 2015 for Cyclone V SoC)
- Low latency and fast response in FPGA logic for motor control loops

HEV/EV System



DRIVING QUALITY DESIGNS

As automotive digital content and control systems move to high definition, wireless communication, and multi-gigabit bandwidths, automakers and system OEMs will continue to demand top-notch quality semiconductor devices. With tens of millions of programmable logic devices shipped to automotive customers worldwide since 2003, we are well positioned for high-volume automotive production.

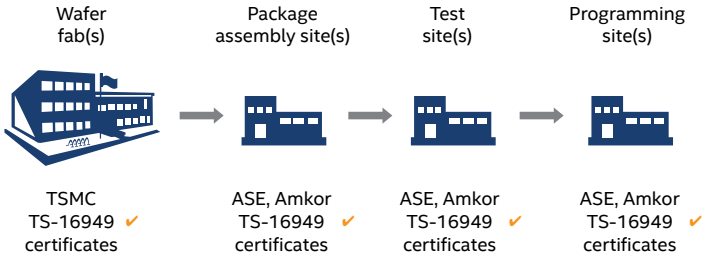
As an active member of the Automotive Electronics Council (AEC), Altera has chaired two AEC subcommittees and qualifies all of its automotive or "A" grade products to the AEC-Q100 standard. Our production part approval process (PPAP) includes the AEC-Q100 qualification results in the document package we provide to qualify your products. The PPAP provides the base-line product details including die, package, wafer fabrication process, package assembly process, and constituent materials.

We have a zero-defect philosophy, with rigorous procedures at each phase of development to ensure the highest quality and lowest defective parts per million (DPPM). Our wafer fabs, package, assembly, test, and programming facilities are TS-16949 certified for a quality management system that provides for continual improvement, emphasizes defect prevention, and reduces variation and waste in the supply chain.

We take business continuity planning (BCP) seriously and employ several initiatives to ensure you have a continuous supply of product, including use of six fabs across four locations, dual fab strategy by Fabmatch methodology, multiple assembly site sourcing, and sub-material sourcing control.

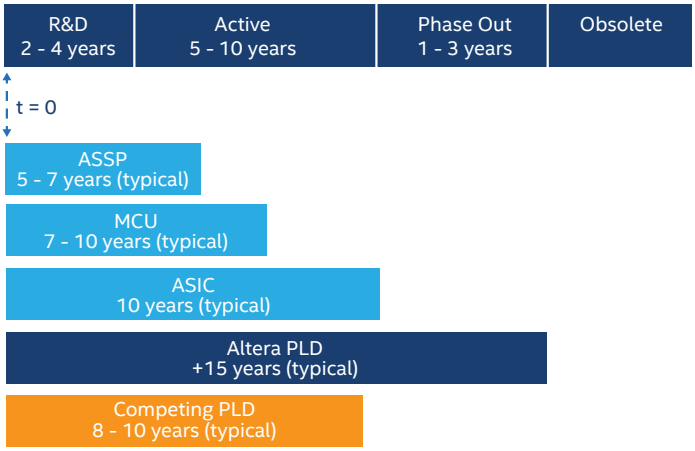
We understand that you need to support your products and vehicles for a minimum of 10 years after release. Our average product cycle is 15 years, with many of our products having lifetimes in excess of 20 years, so you can design in our products with confidence. When change is absolutely mandatory, we take exceptional care to provide special product change notifications so you can manage the delicate rollout of changes to your customers —the automakers—in a coordinated and well-orchestrated manner.

Altera's TS-16949 Compliant Manufacturing Flow



Life Cycle Comparison

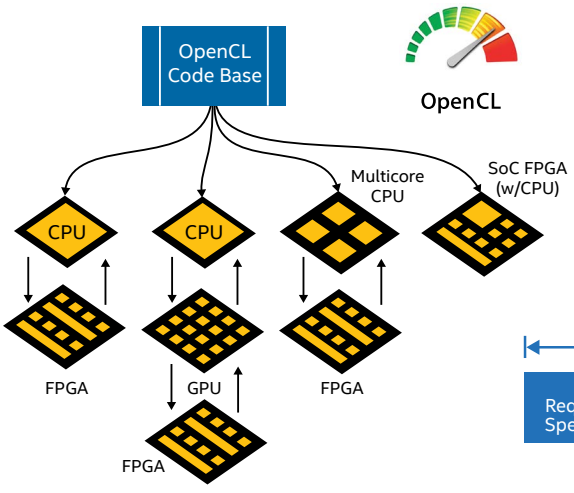
Alignment to application life cycle dynamics



OPENCL DEVELOPMENT FLOW DELIVERS PROTOTYPES IN MINUTES

OpenCL enables FPGAs to be programmed in a C-like language instead of the traditional register transfer level (RTL) programming language. This enables FPGAs to be more accessible to software engineers who traditionally do not use RTL and are more familiar with C-based languages. Using this methodology, software engineers can now target FPGAs to increase performance and flexibility over CPU or GPU-based systems while using significantly less power. This combination of increased performance, flexibility and reduced power is ideal for automotive designs that require semiconductor devices to process huge volumes of data in an energy-efficient fashion. OpenCL design is supported today in Altera's automotive qualified Cyclone V SoC family.

Portability Across Heterogeneous Platforms

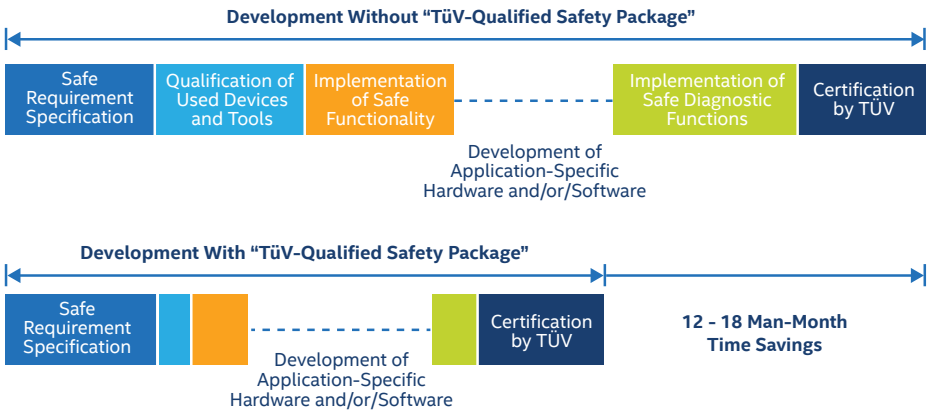


SAFETY FIRST! ALTERA'S LEADERSHIP IN FUNCTIONAL SAFETY EXPANDS TO ISO 26262

The automotive industry is adding multiple active safety systems to reduce the risk of injury and harm. Adapted from the IEC 61508 functional safety standard, the ISO 26262 automotive electronic system safety standard helps you avoid systematic faults and also detect, control, and mitigate any random hardware faults that may cause a malfunction of the system.

To simplify and speed up your certification process, we are working with TÜV Rheinland, an independent third-party assessor specializing in functional safety testing and certification, to receive qualification to ISO 26262. Altera is the first FPGA supplier whose FPGA devices, diagnostics IP, development tools, and FPGA design flow are all certified for the IEC 61508 functional safety standard. Our Functional Safety Data Pack (FSDP) typically saves customers 12-18 man months in certifying their safety applications.

Altera's Cyclone V SoC family will be the first family qualified for ISO 26262 with our Automotive Functional Safety Data Pack (AFSDP). A detailed safety manual and general FMEDA application note are available now to start your design along with a suite of diagnostics IP. Additionally, we are developing a



detailed FMEDA calculator tool to support required hardware architectural metric calculations. Audit and certification are scheduled for mid-2015.

Altera's functional safety approach is a holistic one, which provides guidance in methodology, backed up with qualified tools that increase your tool confidence and may eliminate the use of redundant tool chains. Next, we offer a safety- ready suite of diagnostics IP and expert technical support along with our certified PLDs. Functional safety documentation, reliability reports, and our TÜV certificate will assist you in the certification of your systems. Safety first!

For additional details on our ISO 26262 functional safety program, please visit:

http://www.altera.com/end-markets/auto/safety/aut-safety.html

COMMON AUTOMOTIVE IP – ALTERA AND PARTNER

Altera and its partners offer a broad portfolio of off-the-shelf, configurable IP cores for our devices. This pre-validated IP can help you further accelerate your design flow. Examples include:

INTERFACE IP	
Connectivity	Provider(s)
CAN	Bosch, CAST, IFI
LIN	Bosch, CAST
FlexRay	Bosch
DisplayPort / eDP	Altera / Bitec
PCI Express® (PCIe®)	Altera - MegaCore® function
OpenLDI	Altera - megafunction

GRAPHICS IP	
Function	Provider(s)
Video and Image Processing suite: scaler, converters, Alpha Blender, and more	Altera
2D/3D Graphics, HMIs, Video I/O	TES
Video and graphics	Imagem Technology
DisplayPort / eDP	Altera / Bitec
Video codec	CAST

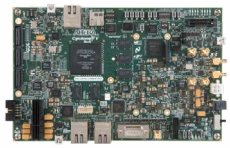
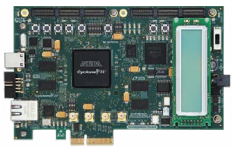
GRAPHIC AND VIDEO IP – PARTNERS

When graphical needs exceed 7-segment or matrix displays, and a dedicated GPU is over-kill, enhanced graphics can be implemented with partner IP in the FPGA fabric. This can range from dedicated functions, such as 3D format conversion, image warping, to full 2D or 3D capable soft GPUs. The table below highlights two examples from the large Altera network of IP providers with unique graphical IP solutions.

FUNCTIONALITY /IP	ATTRIBUTES	PARTNER / BRAND / WEBSITE
• HMI solutions • Video Frame Grabber • Graphics Rendering • ML-Display Controller	• Deployed in >3M vehicles • Small footprint • Low-power GPU	Imagem Technology ATHLET ® www.imagem-technology.com
• HMI System Solutions • 2D / 3D Soft GPUs • Warping • Video IOs, Multiview • 3D Surround View	• IPs • System solutions • Services	TES Electronic Solutions D/AVE, GUILIANI www.tes-dst.com

ALTERA DEVELOPMENT BOARDS

Jump start your prototype with an Altera development board. You can purchase Altera Cyclone FPGA development boards from www.altera.com. Additional boards and daughtercards are available from partners.

FAMILY / DENSITY	PART NUMBER	IMAGE
Cyclone V SX SoC Dual-core ARM Cortex®-A9 processor, 110K LE, 3 Gbps Transceiver	DK-DEV-5CSXC6N/ES	
Cyclone V GT 301K LE, 5 Gbps Transceiver	DK-DEV-5CGTD9N	
Cyclone V E 149K LE	DK-DEV-5CEA7N	
Cyclone IV GX 149.8K LE, 3 Gbps Transceiver	DK-DEV-4CGX150N	
Cyclone IV GX Starter 14.4K LE, 2.5 Gbps Transceiver	DK-START-4CGX15N	
MAX 10 50K LE, ADC	DK-DEV-10M50-A	
MAX 10 8K LE, ADC	EK-10M08E144ES	
MAX V 570 LE	DK-DEV-5M570ZN	

AUTOMOTIVE GRADE PRODUCTS

Our automotive-grade devices feature junction temperature support from -40°C to +125°C (or higher on selected devices). These devices meet or exceed ISO 9001:2001 and AEC-Q100 standards. All our automotive-grade devices are manufactured at fully TS-16949-registered/certified sites using some of programmable logic industry's smallest, highest reliability, and mainstream semiconductor fabrication processes. Our automotive-grade portfolio spans CPLDs to FPGA and also includes SoCs as well as power management PowerSoCs.

INTRODUCING THE CYCLONE V SOC

The Cyclone V SoC integrates an ARM-based hard processor system (HPS) with our FPGA fabric. These user-customizable SoCs increase system performance, lower power consumption, and reduce board space requirements, all designed to help you lower your overall system cost.

Cyclone V SoC key features:

- AEC-Q100 automotive-grade options
- Dual-core ARM Cortex - A9 processors, 700MHz
- Vertical and horizontal migration
- 3 Gbps and 5 Gbps transceiver options
- Hard IP: Dual CAN, Dual EMAC, Dual PCIe
- Safety ready - Error correction code (ECC) support

CYCLONE V SOC PACKAGE / MAXIMUM USER I/O MATRIX

Automotive-grade products are highlighted in yellow. Others are available for auto qualification upon request.

FAMILY	PRODUCT LINE	LOGIC DENSITY (K LES)	PLL FPGA/ HPS (COUNT)	PACKAGE TYPE/ PIN COUNT														
				UBGA-484 (U19)					UBGA-672 (U23)					FBGA-896 (F31)				
				BALL SPACING (MM)														
				0.8					0.8					1.0				
				DIMENSIONS (MM)														
				19 x 19					23 x 23					31 x 31				
				FPGA I/OS / PROCESSOR I/OS / LVDS I/OS / TRANSCEIVERS (XCVR COUNT)														
				FPGA I/O	HPS I/O	LVDS TX	LVDS RX	XCVR	FPGA I/O	HPS I/O	LVDS TX	LVDS RX	XCVR	FPGA I/O	HPS I/O	LVDS TX	LVDS RX	XCVR
Cyclone V SE SoC	5CSE-A2	25	5 / 3	66	151	15	18	–	145	181	31	35	–	–	–	–	–	–
	5CSE-A4	40	5 / 3	66	151	15	18	–	145	181	31	35	–	–	–	–	–	–
	5CSE-A5	85	6 / 3	66	151	15	18	–	145	181	31	35	–	288	181	72	72	–
	5CSE-A6	110	6 / 3	66	151	15	18	–	145	181	31	35	–	288	181	72	72	–
Cyclone V SX SoC (3 Gbps)	5CSX-C2	25	5 / 3	–	–	–	–	–	145	181	31	35	6	–	–	–	–	–
	5CSX-C4	40	5 / 3	–	–	–	–	–	145	181	31	35	6	–	–	–	–	–
	5CSX-C5	85	6 / 3	–	–	–	–	–	145	181	31	35	6	288	181	72	72	9
	5CSX-C6	110	6 / 3	–	–	–	–	–	145	181	31	35	6	288	181	72	72	9
Cyclone V ST SoC (5 Gbps)	5CST-D5	85	6 / 3	–	–	–	–	–	–	–	–	–	–	288	181	72	72	9
	5CST-D6	110	6 / 3	–	–	–	–	–	–	–	–	–	–	288	181	72	72	9

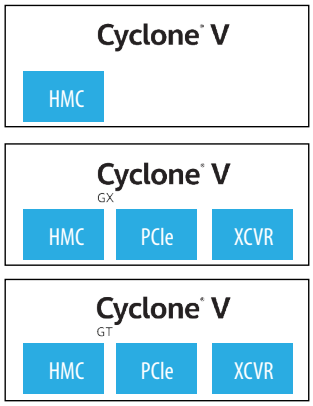
AEC-Q100 Package options available with automotive-grade variants.

CYCLONE V FPGA

Altera's Cyclone V FPGAs provide the industry's lowest system cost and power, along with performance levels that make the device family ideally suited for differentiating your high-volume applications.

Cyclone V FPGA key features:

- Up to 40% power savings over prior generation
- Vertical migration across logic densities
- 3 Gbps and 5 Gbps transceiver options
- PCIe interface (hard IP)
- Memory controller (hard IP)
- Variable-precision DSP blocks
- 4 to 8 Phase-locked loop (PLL)



CYCLONE V PACKAGE / MAXIMUM USER I/O MATRIX

Automotive-grade products are highlighted in yellow. Others are available for auto qualification upon request.

FAMILY	PRODUCT LINE	LOGIC DENSITY (K LES)	PLL (COUNT)	PACKAGE TYPE/ PIN COUNT									
				MBGA -301 (M11)	MBGA -383 (M13)	MBGA -484 (M15)	FBGA -256 (F17)	UBGA -324 (U15)	UBGA -484 (U19)	FBGA -484 (F23)	FBGA -672 (F27)	FBGA -896 (F31)	FBGA -1152 (F35)
				BALL SPACING (MM)									
				0.5	0.5	0.5	1.0	0.8	0.8	1.0	1.0	1.0	1.0
				DIMENSIONS (MM)									
				11 x 11	13 x 13	15 x 15	17 x 17	15 x 15	19 x 19	23 x 23	27 x 27	31 x 31	35 x 35
				I/OS / LVDS / TRANSCEIVERS (COUNT)									
CYCLONE V E	5CE-A2	25	4	–	223/50*	–	128 / 32	176 / 44	224 / 56	224 / 56	–	–	–
	5CE-A4	49	4	–	223/50*	–	128 / 32	176 / 44	224 / 56	224 / 56	–	–	–
	5CE-A5	77	6	–	175/38*	–	–	–	224 / 56	240 / 60	–	–	–
	5CE-A7	149.5	6	–	–	240 / 60	–	–	240 / 60	240 / 60	336 / 84	480 / 120	–
	5CE-A9	301	6	–	–	–	–	–	240 / 122	224 / 56	336 / 84	480 / 120	–
CYCLONE V GX (3 GBPS)	5CGX-C3	35.5	4	–	–	–	–	144 / 36 / 3	208 / 52 / 3	208 / 52 / 3	–	–	–
	5CGX-C4	50	6	129/21*/ 4	175/38*/ 6	–	–	–	224 / 56 / 6	240 / 60 / 6	336 / 84 / 6	–	–
	5CGX-C5	77	6	129/21*/ 4	175/38*/ 6	–	–	–	224 / 56 / 6	240 / 60 / 6	336 / 84 / 6	–	–
	5CGX-C7	149.5	7	–	–	240 / 60 / 3	–	–	240 / 60 / 6	240 / 60 / 6	336 / 84 / 9	480 / 120 / 9	–
	5CGX-C9	301	8	–	–	–	–	–	240 / 60 / 5	224 / 56 / 6	336 / 84 / 9	480 / 120 / 12	560 / 140 / 12
CYCLONE V GT (5 GBPS)	5CGT-D5	77	6	129/21*/ 4	175/38*/ 6	–	–	–	224 / 56 / 6	240 / 60 / 6	336 / 84 / 6	–	–
	5CGT-D7	149.5	7	–	–	240 / 60 / 3	–	–	240 / 60 / 6	240 / 60 / 6	336 / 84 / 9	480 / 120 / 9	–
	5CGT-D9	301	8	–	–	–	–	–	240 / 60 / 5	224 / 56 / 6	336 / 84 / 9	480 / 120 / 12	560 / 140 / 12

AEC-Q100 Package options available with automotive-grade variants.

True LVDS I/O count only. Does not inlcude eTX. *Additional RX available

CYCLONE IV E PACKAGE / MAXIMUM USER I/O MATRIX

Automotive-grade products are highlighted in yellow. Others are available for auto qualification upon request.

FAMILY	PRODUCT LINE	LOGIC DENSITY (K LES)	PLL (COUNT)	PACKAGE TYPE/ PIN COUNT							
				EQFP-144 (E144)	MBGA-164 (M164)	UBGA-256 (U256)	FBGA-256 (F256)	UBGA-484 (U484)	FBGA-324 (F324)	FBGA-484 (F484)	FBGA-780 (F780)
				BALL SPACING (MM)							
				0.5	0.5	0.8	1.0	0.8	1.0	1.0	1.0
				DIMENSIONS (MM)							
				22 x 22	8 x 8	14 x 14	17 x 17	19 x 19	19 x 19	23 x 23	29 x 29
				I/OS / LVDS I/OS (COUNT)							
Cyclone IV E	EP4CE6	6.3	2	91 / 21	–	179 / 66	179 / 66	–	–	–	–
	EP4CE10	10.3	2	91 / 21	–	179 / 66	179 / 66	–	–	–	–
	EP4CE15	15.4	4	81 / 18	74 / 21	165 / 53	165 / 53	346 / 140	–	343 / 137	–
	EP4CE22	22.3	4	79 / 17	–	153 / 52	153 / 52	–	–	–	–
	EP4CE30	28.8	4	–	–	–	–	–	193 / 61	328 / 124	532 / 224
	EP4CE40	39.6	4	–	–	–	–	328 / 124	193 / 61	328 / 124	532 / 224
	EP4CE55	55.9	4	–	–	–	–	324 / 132	–	324 / 132	374 / 160
	EP4CE75	75.4	4	–	–	–	–	292 / 110	–	292 / 110	426 / 178
	EP4CE115	114.5	4	–	–	–	–	–	–	280 / 103	528 / 230

AEC-Q100 Package options available with automotive-grade variants.

LVDS count includes dedicated and emulated LVDS pairs, see Cyclone IV Device Handbook.

CYCLONE IV GX PACKAGE / MAXIMUM USER I/O MATRIX

Automotive-grade products are highlighted in yellow. Others are available for auto qualification upon request.

FAMILY	PRODUCT LINE	LOGIC DENSITY (K LES)	PLL (COUNT)	PACKAGE TYPE/ PIN COUNT																
				QFN-148 (N148)			FBGA-169 (F169)			FBGA-324 (F324)			FBGA-484 (F484)			FBGA-672 (F672)			FBGA-896 (F896)		
				BALL SPACING (MM)																
				0.5			1.0			1.0			1.0			1.0			1.0		
				DIMENSIONS (MM)																
				11 x 11			14 x 14			19 x 19			23 x 23			27 x 27			31 x 31		
				I/OS / LVDS / TRANSCEIVERS (COUNT)																
				I/O	LVDS	XCVR	I/O	LVDS	XCVR	I/O	LVDS	XCVR	I/O	LVDS	XCVR	I/O	LVDS	XCVR	I/O	LVDS	XCVR
CYCLONE IV GX (2.5/ 3 GBPS)	EP4CGX15	14.4	3	72	25	2	72	25	2	–	–	–	–	–	–	–	–	–	–	–	–
	EP4CGX22	21.3	4	–	–	–	72	25	2	150	64	4	–	–	–	–	–	–	–	–	–
	EP4CGX30	29.4	4 / 6	–	–	–	72	25	2	150	64	4	290	130	4	–	–	–	–	–	–
	EP4CGX50	49.9	8	–	–	–	–	–	–	–	–	–	290	130	4	310	140	8	–	–	–
	EP4CGX75	73.9	8	–	–	–	–	–	–	–	–	–	290	130	4	310	140	8	–	–	–
	EP4CGX110	109.4	8	–	–	–	–	–	–	–	–	–	270	120	4	393	181	8	475	220	8
	EP4CGX150	149.8	8	–	–	–	–	–	–	–	–	–	270	120	4	393	181	8	475	220	8

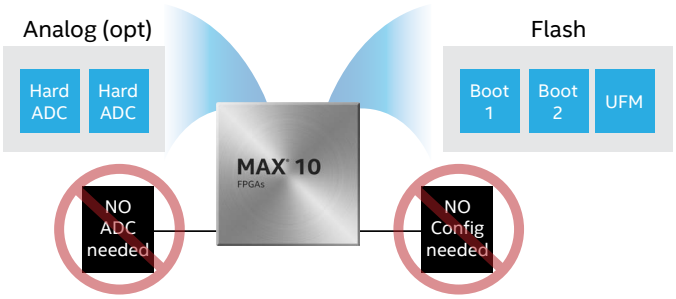
AEC-Q100 Package options available with automotive-grade variants.

INTRODUCING THE MAX10 FPGA (2.5V, 1.2V CORE)

Altera's new MAX® 10 FPGAs revolutionize non-volatile integration by delivering advanced processing capabilities in a low-cost, instant-on, small form factor programmable logic device.

MAX 10 FPGA key features:

- 2 to 50k LE logic density
- Dual-image configuration
- Instant-on configuration
- Dual or single core rail options
- Optional ADC converter(s)
- Variable-precision DSP blocks



MAX 10 FPGA DUAL (CORE) SUPPLY DEVICE PACKAGE / MAXIMUM USER I/O MATRIX

Automotive-grade products are highlighted in yellow. Others are available for auto qualification upon request.

FAMILY	PRODUCT LINE	LOGIC DENSITY (K LES)	PLL (COUNT)	PACKAGE TYPE/ PIN COUNT					
				36-WLCSP (V36)*	81-WLCSP (V81)*	256-FBGA (F256)	324-UBGA (U324)	484-FBGA (F484)	672-FBGA (F672)
				PAD / BALL SPACING (MM)					
				0.4	0.4	1.0	0.8	1.0	1.0
				DIMENSIONS (MM)					
				3 x 3	4 x 4	17 x 17	15 x 15	23 x 23	27 x 27
				MAXIMUM IOS - TRUE RX / TRUE TX / EMULATED TX (COUNT)					
				IOs - RX / TX / eTX	IOs - RX / TX/ eTX	IOs - RX / TX / eTX	IOs - RX / TX / eTX	IOs - RX / TX / eTX	IOs - RX / TX / eTX
MAX 10 FPGA "D"	10M02D	2	1*/2	27 - 7/3/7	–	–	160 - 47/9/47	–	–
				C			**C, C_6**		
	10M04D	4	2	–	–	178 - 54/13/54	246 - 81/15/81	–	–
						C **A**	**C** A		
	10M08D	8	1*/2	–	56 - 17/7/17	178 - 54/13/54	246 - 81/15/81	250 - 83/15/83	–
					C F	**C** **A**	**C**, C_6 A	C, C-6 A	
	10M16D	16	4	–	–	178 - 54/13/54	246 - 81/15/81	320 - 116/22/116	–
						C **A**	**C**, C_6 A	C, C_6 A	
	10M25D	25	4	–	–	178 - 54/13/54	–	360 - 136/24/136	–
						C **A**		C, C_6 A	
	10M40D	40	4	–	–	178 - 54/13/54	–	360 - 136/24/136	500 - 192/30/192
						C **A**		C, C_6 A	C A
	10M50D	50	4	–	–	178 - 54/13/54	–	360 - 136/24/136	500 - 192/30/192
						C **A**		C, C_6 A	C A

Note: Feature set options: C = Base, F = Dual Configuration CFM, A = Dual Configuration CFM + Analog Features

Note: RX = True LVDS RX, TX = True LVDS TX, eTX = emulated LVDS TX, additional LOW SPEED eTX/RX IO provided.

Note: "_6" denotes special FAST speed grade supported, A6G suffix. Contact Factory on availability.

AEC-Q100 Package options available in Quartus II with automotove-grade variants.

AEC-Q100 Planned package option - available upon request / approval. A-Grade production 2H2015-1H2016 - device dependent. See Website for updated information.

MAX 10 FPGA SINGLE (CORE) SUPPLY DEVICE PACKAGE / MAXIMUM USER I/O MATRIX (3.0V OR 3.3V CORE)

Automotive-grade products are highlighted in yellow. Others are available for auto qualification upon request.

FAMILY	PRODUCT LINE	LOGIC DENSITY (K LES)	PLL (COUNT)	PACKAGE TYPE/ PIN COUNT		
				144-EQFP (E144)	153-MBGA (M153)	169-UBGA (U169)
				PAD / BALL SPACING (MM)		
				0.5	0.5	0.8
				DIMENSIONS (MM)		
				22 x 22	8 x 8	11 x 11
				MAXIMUM IOS - TRUE RX / TRUE TX / EMULATED TX (COUNT)		
				IOs - RX / TX / eTX	IOs - RX / TX / eTX	IOs - RX / TX / eTX
MAX 10 FPGA "S"	10M02S	2	1	101 - 27/7/27	112 - 29/9/29	130 - 38/9/38
				C	C	C
	10M04S	4	1	101 - 27/10/27	112 - 29/9/29	130 - 38/9/38
				C A	C A	C A
	10M08S	8	1	101 - 27/10/27	112 - 29/9/29	130 - 38/9/38
				C A	C A	C A
	10M16S	16	1	101 - 27/10/27	–	130 - 38/9/38
				C A		C A
	10M25S	25	1	101 - 27/10/27	–	–
				C A		
	10M40S	40	1	101 - 28/10/28	–	–
				C A		
	10M50S	50	1	101 - 28/10/28	–	–
				C A		

Note: Feature set options: C = Base, F = Dual Configuration CFM, A = Dual Configuration CFM + Analog Features

Note: RX = True LVDS RX, TX = True LVDS TX, eTX = emulated LVDS TX, additional LOW SPEED eTX/RX IO provided.

AEC-Q100 Package options available in Quartus II with automotove-grade variants.

AEC-Q100 Planned package option - available upon request / approval. A-Grade production 2H2015-1H2016 - device dependent. See Website for updated information.

MAX V (CPLD) DEVICE PACKAGE / MAXIMUM USER I/O MATRIX

Automotive-grade products are highlighted in yellow. Others are available for auto qualification upon request.

FAMILY	PRODUCT LINE	LOGIC DENSITY (LES)	PACKAGE TYPE/ PIN COUNT							
			MBGA-64 (M64)	EQFP-64 (E64)	MBGA-68 (M68)	TQFP-100 (T100)	MBGA-100 (M100)	TQFP-144 (T144)	FBGA-256 (F256)	FBGA-324 (F324)
			BALL SPACING (MM)							
			0.5	0.4	0.5	0.5	0.5	0.5	1.0	1.0
			DIMENSIONS (MM)							
			4.5 x 4.5	9 x 9	5 x 5	16 x 16	6 x 6	22 x 22	17 x 17	19 x 19
			I/OS (COUNT)							
MAX V	5M40Z	40	30	54	–	–	–	–	–	–
	5M80Z	80	30	54	52	79	–	–	–	–
	5M160Z	160	–	54	52	79	79	–	–	–
	5M240Z	240	–	–	52	79	79	114	–	–
	5M570Z	570	–	–	–	74	74	114	159	–
	5M1270Z	1270	–	–	–	–	–	114	211	271
	5M2210Z	2210	–	–	–	–	–	–	203	271

AEC-Q100 Package options available with automotive-grade variants.

Notes:

1. For a specific list of part numbers for automotive-grade devices, consult the Automotive-Grade Device Handbook at altera.com.
2. For details on additional product line features (i.e., hard IP blocks, on-chip memory, and so on), consult the online device handbook at altera.com
3. Other automotive-grade options might be available upon request. Consult your Altera sales representative to submit your request.
4. For full specifications, features, and I/O count for GPIO, HPS, LVDS, emulated LVDS, and transceivers, refer to Quartus II software documentation/handbooks.

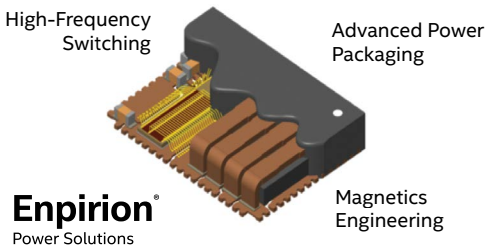
POWERING YOUR INNOVATION: AUTOMOTIVE-GRADE ENPIRION POWERSOCS

Altera's automotive-grade Enpirion PowerSoC power management products are ideally suited for powering automotive-grade programmable logic devices and other automotive sub-system circuits. These highly integrated devices combine high efficiency and a tiny footprint to maximize power density while minimizing heat. With a 45,000 years mean time between failures (MTBF), Enpirion PowerSoCs are built to meet automotive reliability requirements.

Enpirion PowerSoC key features:

- AEC-Q100 qualified
- 45,000 years MTBF
- Integrated MOSFETs, inductor, and capacitors enable tiny footprint
- High efficiency reduces power loss and heat
- Easy to use with minimal external components, comprehensive FPGA power tools, and fully validated designs

Key Technology Enablers of High-density PowerSoC



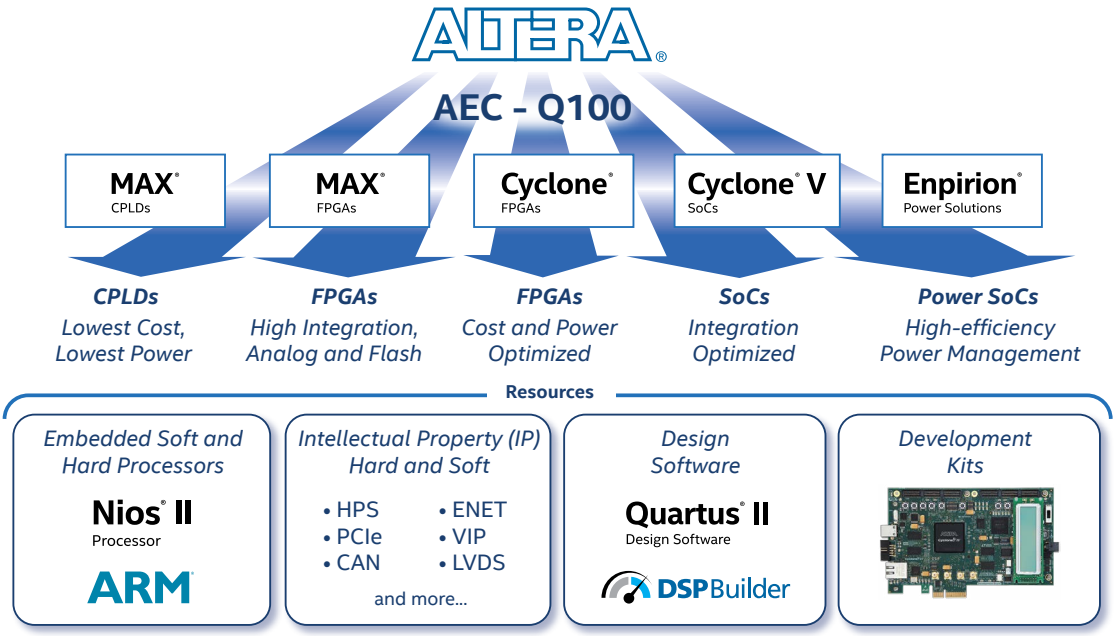
ENPIRION AUTOMOTIVE-GRADE POWERSOC MATRIX

Automotive-grade products are highlighted in yellow. Others are available for auto qualification upon request.

PRODUCTS	I_{OUT} (A)	V_{IN} RANGE (V)	V_{OUT} RANGE (V)	PACKAGE	APPROX. TOTAL SOLUTION SIZE (MM^2)	ENABLE	OVERCURRENT PROTECTION (OCP)	OVER-TEMPERATURE PROTECTION (OTP)	UNDER VOLTAGE LOCK-OUT (UVLO)	VID V_{OUT} SET	EXTERNAL VOLTAGE DIVIDER V_{OUT} SET	POWER GOOD (POK)	PROGRAMMABLE SOFT-START	FREQUENCY SYNCHRONIZATION	PARALLEL OPERATION
EP53xx 5V PowerSoCs															
EP5358LUA	0.6	2.4 – 5.5	0.60 – (V_{IN} - $V_{DROPOUT}$)	uQFN16	14	•	•	•	•	•	•				
EP5358HUA	0.6	2.4 – 5.5	1.8 – 3.3	uQFN16	14	•	•	•	•	•					
EP53A8LQA	1.0	2.4 – 5.5	0.60 – (V_{IN} - $V_{DROPOUT}$)	QFN16	21	•	•	•	•	•	•				
EP53A8HQA	1.0	2.4 – 5.5	1.8 – 3.3	QFN16	21	•	•	•	•	•					
EN63xx 5V Efficiency-Optimized PowerSoCs															
EN6310QA	1.0	2.7 – 5.5	0.6 – 3.3	QFN30	65	•	•	•	•		•	•	•		
EN6337QA	3.0	2.5 – 6.6	0.75 – (V_{IN} - $V_{DROPOUT}$)	QFN38	75	•	•	•	•		•	•	•	•	
EN6347QA	4.0	2.5 – 6.6	0.75 – (V_{IN} - $V_{DROPOUT}$)	QFN38	75	•	•	•	•		•	•	•	•	
EN6360QA	8.0	2.5 – 6.6	0.60 – (V_{IN} - $V_{DROPOUT}$)	QFN60	190	•	•	•	•		•	•	•	•	•
EN63A0QA	12.0	2.5 – 6.6	0.60 – (V_{IN} - $V_{DROPOUT}$)	QFN76	227	•	•	•	•		•	•	•	•	•

Note: OCP = Overcurrent protection, OTP = Over-Temperature protection

See device datasheet for more information



Visit our website for information on legacy automotive-grade devices:

- Cyclone III FPGAs
- Cyclone II FPGAs
- Cyclone FPGAs
- MAX II CPLDs
- MAX 7000A CPLDs

WANT TO DIG DEEPER?

To learn more about Altera's automotive-grade products, contact your local FAE or sales representative. You can download automotive handbooks, white papers, and application notes at **www.altera.com/automotive.**

Visit: **www.altera.com/automotive**.

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