Implementing Audio IP in SDI II on Arria V Development Board

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This document describes a reference design that uses the Audio Embed, Audio Extract, Clocked Audio Input and Clocked Audio Output IP with the Serial Digital Interface II (SDI II) MegaCore function to demonstrate the following operations:

- Embed audio in video signal using the SDI II MegaCore function.
- Extract audio signal from the SDI signal.
- Convert Avalon-ST audio data to AES audio format using the Clocked Audio Output IP.
- Convert AES audio data to Avalon-ST format using the Clocked Audio Input IP.
- Embed and extract audio data in NTSC and PAL formats for SD, HD, 3GA and 3GB.

This reference design runs on the Arria V GX development board with an HSMC daughter card.

Functional Description

This section describes the components, and the clock domains and data paths in the reference design.
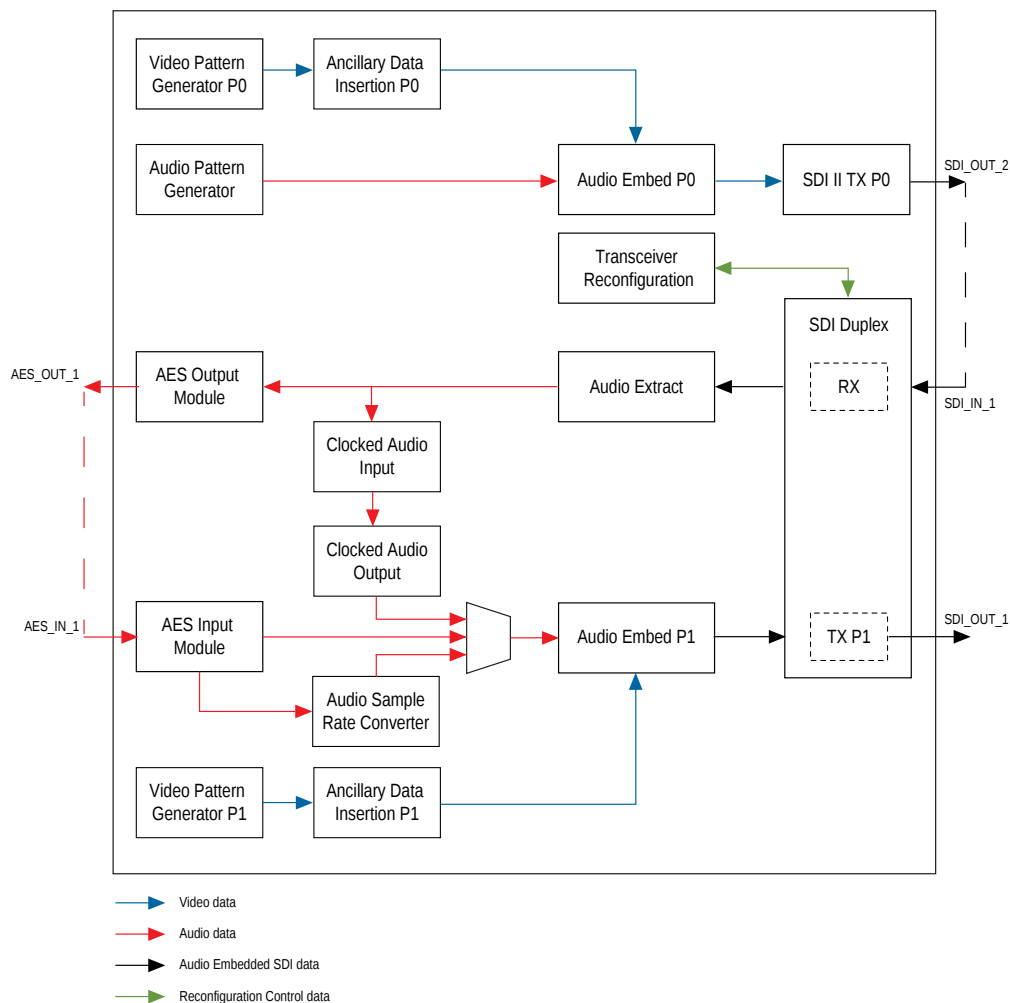
Reference Design Block Diagram

The following diagram show the components of the reference design block diagram.

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Figure 1: Block Diagram

Clock Domain and Data Paths

The following figures show the clock domain and data paths for the SDI channels.

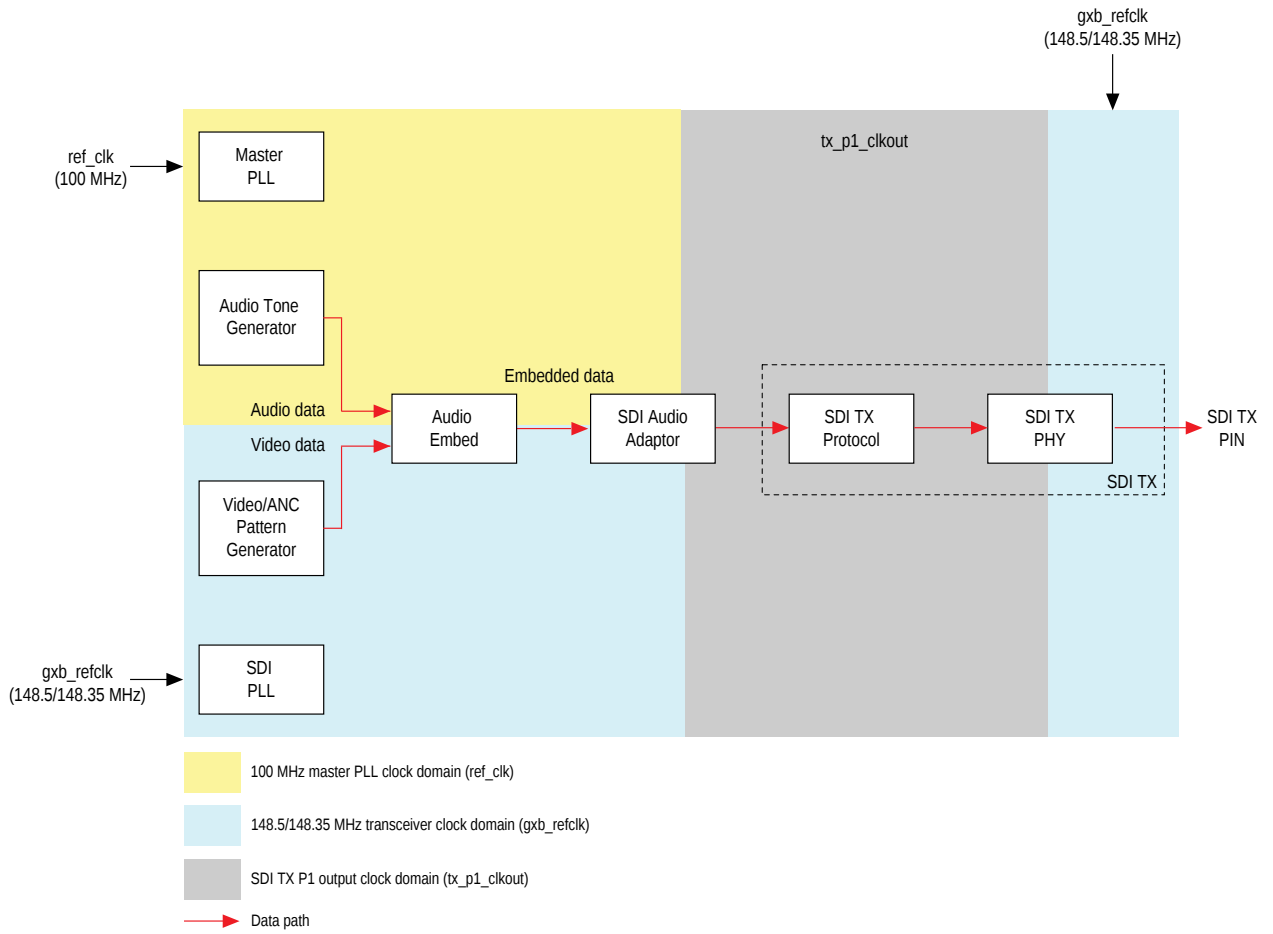**Figure 2: Clock Domain and Data Path for SDI Transmitter Channel**

Figure 3: Clock Domain and Data Path for SDI Duplex Channel
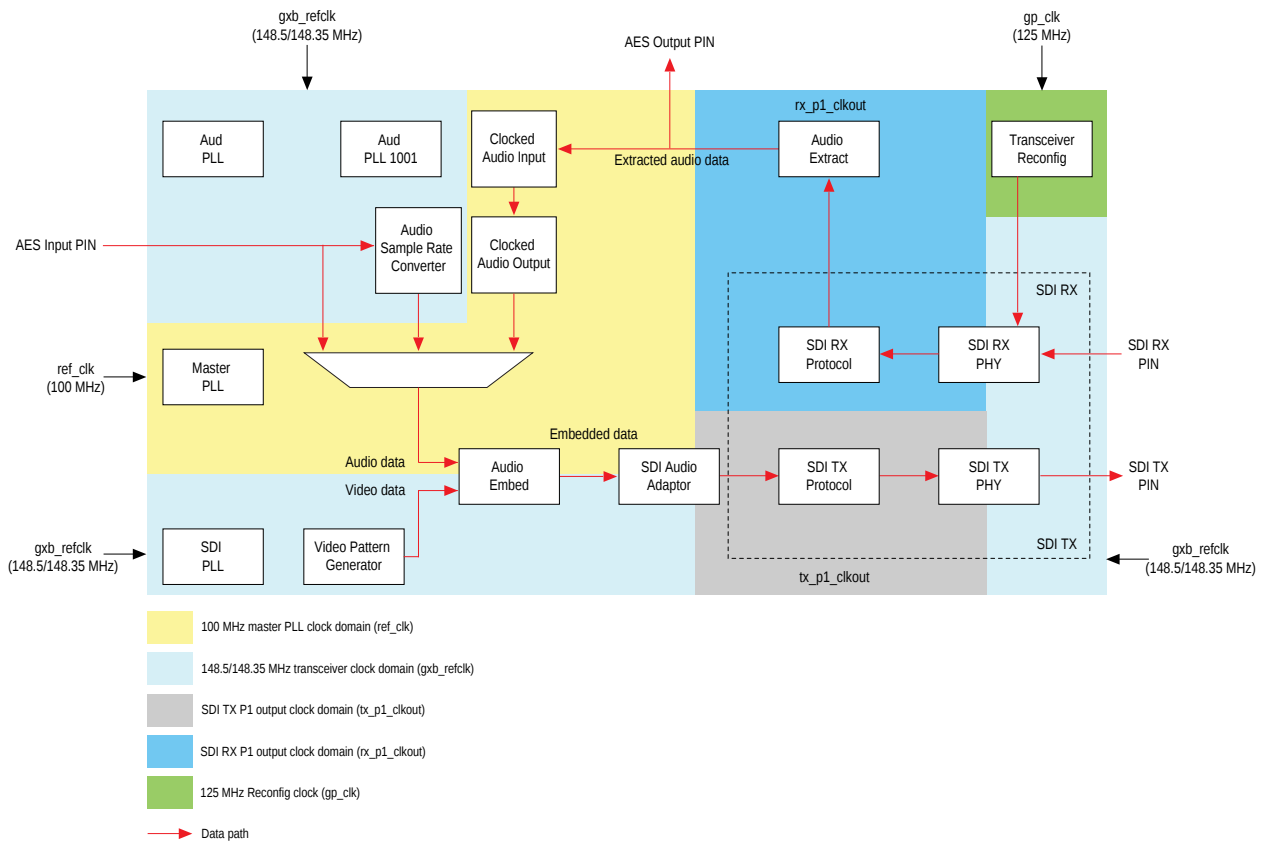
Reference Design Components

The following sections describe the components in the reference design.

Audio Embed

The Audio Embed IP embeds the audio data into SD, HD, and 3G SDI. The input can be either synchronous or asynchronous to the video. However, the audio pairs embedded together in the same audio group must be synchronous to each other.

Audio Extract

The Audio Extract IP extracts the audio data from SD, HD, and 3G SDI. It can extract one channel pair of SD, HD, or 3G embedded audio. To extract more than one channel pair, multiple instances of the IP are required.

Clocked Audio Input

The Clocked Audio Input IP converts the AES clocked audio to the Avalon-ST format.

Clocked Audio Output

The Clocked Audio Output IP accepts the clocked Avalon-ST audio and converts it to AES formats.

Audio Sample Rate Converter

The Audio Sample Rate Converter changes the audio sample rate without affecting the phase or quality. This conversion is required for the Audio Embed IP to embed the audio from different sources with asynchronous clocks domain that run at a different sample rate.

SDI II Transmitter

The triple-standard SDI II transmitter generates the embedded audio SDI signal in SD, HD, or 3G standard. The transmitter sends the audio signal in either NTSC or PAL format.

SDI II Duplex Transceiver

The triple-standard SDI II MegaCore function receives data in SD-SDI, HD-SDI, or 3G-SDI standard and performs receiver-to-transmitter loopback. The transceiver decodes, buffers, recodes, and then transmits the received data. The data can be in either NTSC or PAL format.

Transceiver Reconfiguration

The Transceiver reconfiguration control logic is required for the triple standard handling. This control logic reconfigures the receiver of the duplex core for different incoming SDI data rates.

Video Pattern Generator

The video pattern generator generates the video pattern for different video formats such as 2.970-Gbps 1080p, 1.485-Gbps 1080i and 270-Mbps video patterns. The video test pattern is 100% color bar.

Ancillary Data

This block inserts the ancillary data into the generated video pattern. The ancillary data inserted includes Check Sum Word (CS), Data Count Word (DC) and Data Identification Word (DID/SDID).

Audio Tone Generator

The audio tone generator generates the audio information using an incrementing counter. This audio data cannot be translated into any audible sound. The data is for the audio pattern observation in the audio bar using the SDI signal analyzer in embedded audio mode in an increasing manner. If you want to test using audible audio data, you can use the test audio sine wave pattern in the Audio Embed IP.

SDI Audio Adaptor

The SDI audio adaptor synchronizes the audio embedded SDI data between different clock domains.

Related Information

- **Serial Digital Interface (SDI) User Guide**
  For more information about Audio Embed, Audio Extract, Clocked Audio Input, and Clocked Audio Output IPs, refer to the *Serial Digital Interface (SDI) User Guide*.

- **Audio Sample Rate Converter**
  For more information about the audio sample rate converter, refer to Audio Sample Rate Converter page.

- **Altera Transceiver PHY IP Core User Guide**
  For more information about transceiver reconfiguration, refer to the Transceiver Reconfiguration Controller section in the *Altera Transceiver PHY IP User Guide*.

Getting Started

This section describes the requirements and the procedure to run the reference design.

Hardware and Software Requirements

You need the following hardware and software to run this reference design:

- Arria V GX FPGA development kit
- SDI HSMC daughter card
- Quartus II software, version 13.1
- 3 BNC cables

Hardware Setup

The following figures show the setup of an Arria V FPGA development kit and an SDI HSMC daughter card.

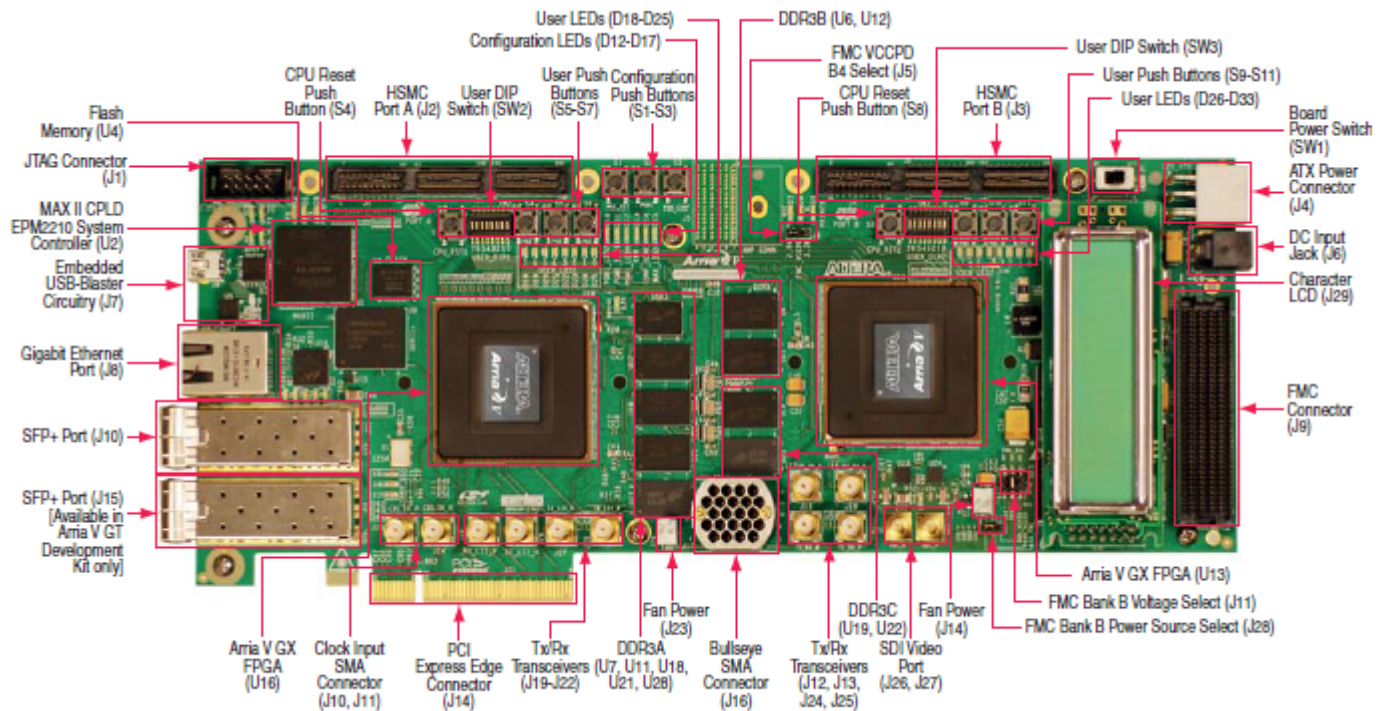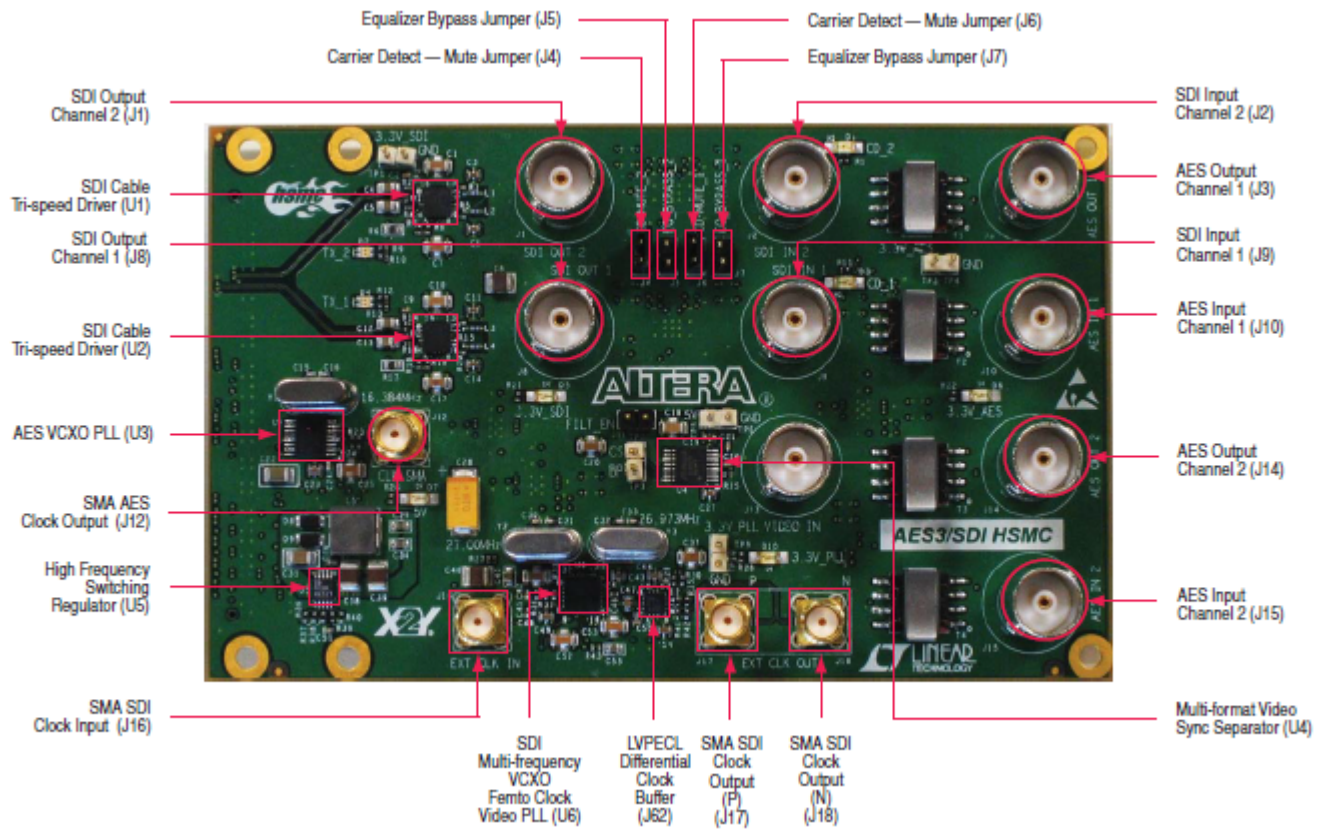**Figure 4: Arria V FPGA Development Kit**

Figure 5: SDI HSMC Daughter Card

Functions on the Arria V GX Development Kit

The following tables describe the function of each user LED, user-defined DIP switch control, and push buttons on the Arria V GX development kit.

Table 1: Functions of LEDs

Bit	Board Reference	Description
7	D33	RX Standard (rx_std[1])
6	D32	RX Standard (rx_std[0])
5	D31	RX Frame Lock (rx_status[4])
4	D30	RX Recovered Clock Hearbeat
3	D29	Audio Extract: Audio Group 4 Present
2	D28	Audio Extract: Audio Group 3 Present
1	D27	Audio Extract: Audio Group 2 Present
0	D26	Audio Extract: Audio Group 1 Present

Table 2: Functions of DIP Switch Controls

Bit	Board Reference	Description
7	SW3.8	Unused
6	SW3.7	Unused
5	SW3.6	Unused
4	SW3.5	1: Indicate the incoming video is in NTSC format (1/1.001 data rate) 0: Indicate the incoming video is in PAL format
3	SW3.4	1: Loopback audio data passing through sample rate converter 0: Loopback audio data depending on setting in DIP switch bit 2 (SW3.3)
2	SW3.3	1: Audio data looped back internally through Clocked Audio Input and Clocked Audio Output IPs 0: Audio data looped back externally without going through converted sample rate
1	SW3.2	Indicates the SDI video standard:
0	SW3.1	00: SD 01: HD 10: 3GB 11: 3GA

Table 3: Functions of Push Buttons

Push Button	Description
PB0	Reset
PB1	Unused
PB2	Unused

Running the Reference Design

To run the reference design, do the following steps.

1. Set up the board connections.
   a. Connect the SDI HSMC to the HSMC Port B of FPGA development board.
   b. Specify the following board settings located on the back of the FPGA development board:

- DIP Switch Bank
- JTAG Chain Header Switch Controls

c. Match the board settings to the settings in the following tables.

Table 4: Settings for DIP Switch Controls

Switch	Schematic Signal Name	Description	Default
1	CLK_SEL	ON: 100 MHz clock select OFF: SMA input clock select	OFF
2	CLK_ENABLE	ON: On-board oscillators enable OFF: On-board oscillators disable	ON
3	FACTORY_USER1	ON: Load factory design from flash for Arria V FPGA 1 at power up OFF: Load user design from flash at power up	ON
4	FACTORY_USER2	Unused	OFF

Table 5: Settings for JTAG Chain Header Switch Controls

Switch	Schematic Signal Name	Description	Default
1	HSMA_JTAG_EN	ON: Bypass HSMA OFF: HSMA in-chain	ON
2	HSMB_JTAG_EN	ON: Bypass HSMB OFF: HSMB in-chain	ON
3	PCIE_JTAG_EN	ON: Bypass FMC connector OFF: FMC connector in-chain	ON
4	NC	Unused	OFF

d. Connect the FPGA development board to the power supply.

2. Download the design file, **a5_sdi_audio_top.qar**, and save it in your local drive.
3. Launch the Quartus II software and click on **a5_sdi_audio_top.qar** to un-archive the QAR file.
4. Regenerate all the Megawizard-generated Verilog design file inside the **megacore_build** folder.
5. Run Qsys to regenerate **audio_loop.qsys**
6. Compile the reference design.
   a. On the File menu, click **Open Project**, navigate to \<*directory*>**a5_sdi_audio_top.qpf** and click **Open**.
   b. On the **Processing** menu, click **Start Compilation**.
7. Download the Quartus II-generated SRAM Object File (**.sof**), \<*directory*>**a5_sdi_audio_top.sof**.
   a. Connect the USB cable to the board's USB connector.

    b. On the **Tools** menu, click **Programmer** to download *<directory>***a5_sdi_audio_top.sof** to the board. The software automatically detects the file during compilation and it appears on the pop-up window.

    c. Select Device 2 in the FPGA development board to be the target of the programming.

    d. Click **Start** to download the file to the board. If the file does not appear in the pop-up windows, click **Add File**, navigate to *<directory>***a5_sdi_audio_top.sof** and click **Open**.

    e. Reload each time after you power up the board because this design is volatile.

When you have successfully set up the board, you can run the different variants discussed in the following sections.

Testing Audio Loopback

Only the SDI duplex instance loops back the audio into the transmitter. The SDI duplex instance is able to loop back because it has both the video pattern generator and the transmitter in the same clock domain. If you want to perform a parallel loopback for the data received from another clock domain to this transmitter, you need a voltage controlled crystal oscillator (VCXO) to synchronize the data between the two clock domains. To test the audio loopback, do the following steps.

1. Connect an SDI signal generator with an embedded audio or SDI OUT 2 to the receiver SDI IN1.
2. Connect an SDI signal analyzer with the embedded audio enabled to the transmitter SDI OUT1.
3. Connect the AES OUT 1 to AES IN 1 using the BNC cable for the audio data external loopback.
4. Switch between the different video standards (SD, HD, 3GA or 3GB) by controlling user2 DIP switch, as indicated in **Table 2**.
5. Check the video pattern result in the SDI signal analyzer.
6. When you enable the embedded audio input in the SDI signal analyzer, you can observe the audio embedded in the following groups:

    a. SD standard: Group 1

    b. HD standard: Groups 1 and 2

    c. 3GA standard: Groups 1, 2, and 3

    d. 3GB standard: Groups 1, 2, 3, and 4

7. Check the audio pattern result using the embedded audio SDI signal analyzer.
8. You can select the audio data to be embedded in SDI OUT1 from the internal loopback through the Clocked Audio Input and Clocked Audio Output paths, the external loopback without the sample rate converter, or the external loopback through the sample rate converter as indicated in **Table 2**.

> **Note:** Take note that in this reference design, the received audio embedded SDI data and the transmitter clock domain in the SDI duplex instance are in the same clock domain . You can transmit the looped back audio data into the audio embed block directly without going through the sample rate converter. If the received audio embedded SDI data and the transmitter in the SDI duplex instance are in different clock domains, you must pass the audio data through the sample rate converter before transmitting to the audio embed block.

Testing the SDI Transmitter with Embedded Audio

To test the SDI transmitter with an embedded audio, do the following steps.

1. Connect an SDI signal analyzer to the transmitter output of SDI OUT2.
2. Switch between the different video standard (SD, HD, 3GA or 3GB) by controlling user2 DIP switch.
3. Check the video pattern result in the SDI signal analyzer.
4. When you enable the embedded audio input in the SDI signal analyzer, you can observe the audio embedded in the following groups:
   a. SD standard: Group 1
   b. HD standard: Groups 1 and 2
   c. 3GA standard: Groups 1, 2, and 3
   d. 3GB standard: Groups 1, 2, 3, and 4
5. Check the audio pattern result using the embedded audio SDI signal analyzer.

Testing AES Audio Extraction

To test if the AES audio is extracted correctly, do the following steps.

1. Connect an SDI signal generator with an embedded audio or SDI OUT 2 to the receiver SDI IN1.
2. Connect AES OUT 1 to the AES input of the audio signal analyzer.
3. Switch between the different video standards (SD, HD, 3GA or 3GB) by controlling user2 DIP switch, as indicated in **Table 2**.
4. When you enable the AES audio input in the audio signal analyzer, you can observe the audio data in the AES format.
5. Check the audio data in the audio signal analyzer.

Table 1: Document Revision History

Date	Version	Changes
December 2013	2013.12.20	First published.
April 2014	2014.04.25	Added link to the design files.

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