How to insert an LVDS buffer between an Altera_PLL and ALTLVDS_RX and ALTLVDS_TX megafunction in external pll mode for Cyclone® V, Arria® V and Stratix® V devices.

Introduction

In the Quartus® II software version 12.1 and onwards you will encounter an error at the Analysis and Synthesis stage when using ALTLVDS (RX and TX) in external PLL mode and either of the following options are turned on in the PLL:

- Enable dynamic reconfiguration of PLL
- Enable access to dynamic phase shift ports

The following guide will describe how to fix this error for Cyclone V, Arria V and Stratix V devices.

1. Set Up

The examples in this document use the following:

- Quartus II software version12.1
- Altera_PLL, ALTLVDS_RX and ALTLVDS_TX megafunctions

2. Background

Figure 2-1 shows the typical connection when using ALTLVDS megafunction in external PLL mode.

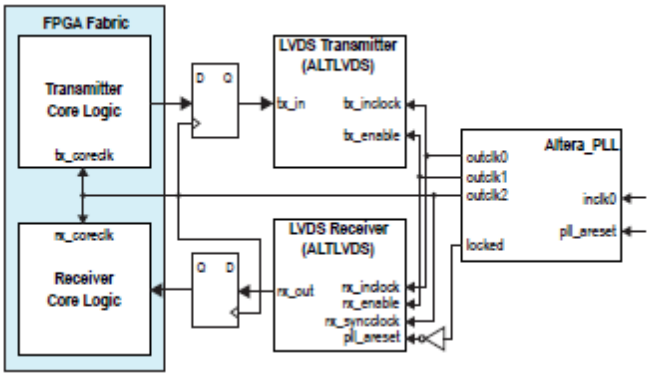

Figure 2-1. LVDS Interface with the Altera_PLL Megafunction (Without DPA and Soft-CDR Mode)

Figure 2-2 shows enabling of dynamic reconfiguration or dynamic phase shifting in the Altera _PLL megafunction.

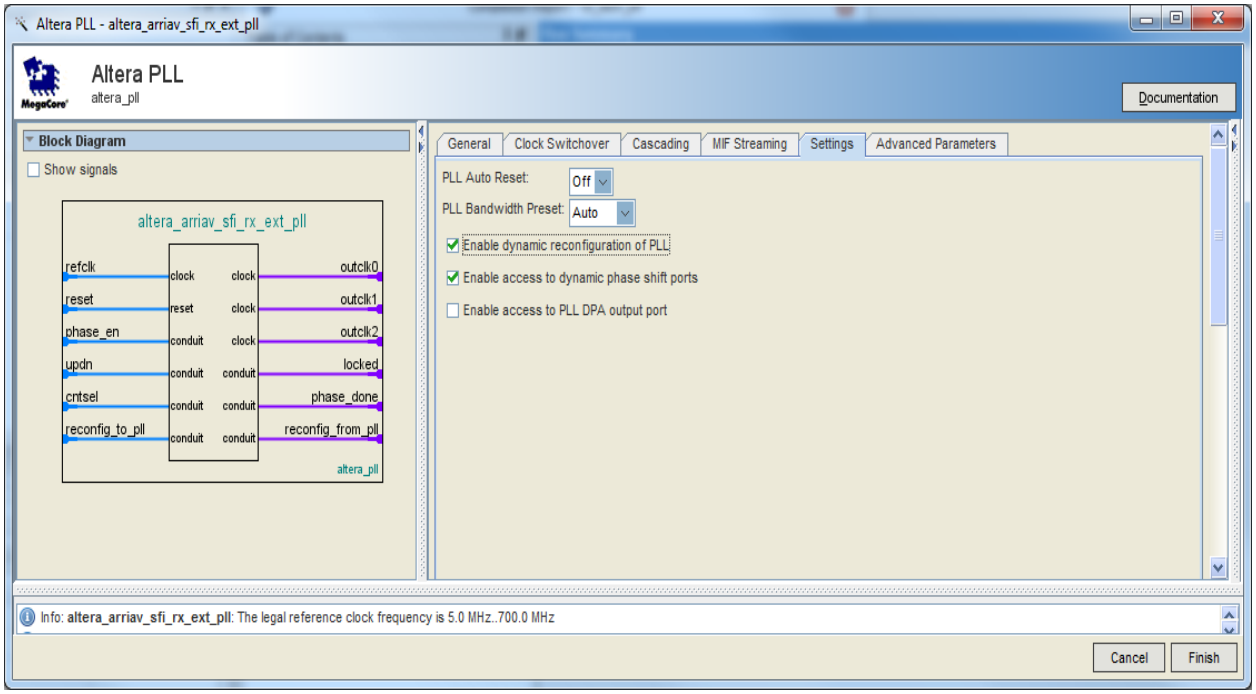

Figure 2-2. Altera_PLL megafunction with Enable dynamic reconfiguration of PLL or Enable access to dynamic phase shift ports turned ON.

The error message seen at the Analysis and Synthesis stage will be dependent of the device family used. The next section covers the workaround for the Arria V, Cyclone V and Stratix V device families.

3. Arria V Devices

In the Quartus II software version 12.1 and onwards the connection shown below will produce two sets of error messages, one for the RX and one for the TX.

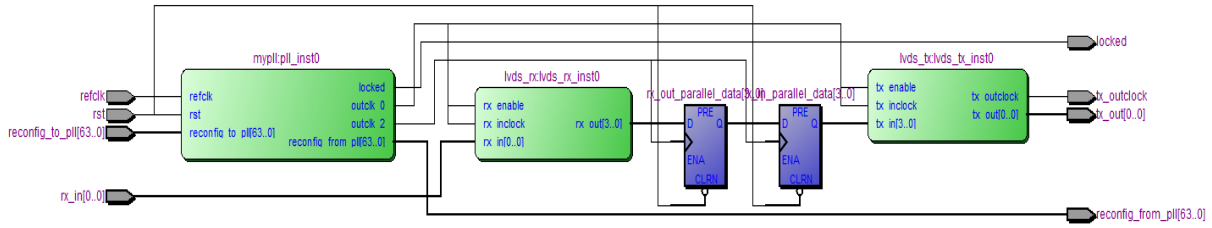

Figure 3-1. LVDS Interface with the Altera_PLL megafunction (Without DPA and Soft-CDR Mode) in Arria V devices

ERROR messages produced by Mapper for ALTLVDS_RX in external PLL mode

Error: SERDES DPA Block node 'lvds_rx:lvds_rx_inst0|altlvds_rx:ALTLVDS_RX_component|lvds_rx_lvds_rx:auto_generated|lvds_rx_dpa3' is not properly connected on the 'RXFCLK' port. It must be connected to one of the valid ports listed below.

Info: Can be connected to LVDSCLK port of arriav_pll_lvds_output WYSIWYG
Info: Can be connected to OUTCLK port of generic_pll WYSIWYG

ERROR messages produced by Mapper for ALTLVDS_TX in external PLL mode

Error: SERDES DPA Block node 'lvds_tx:lvds_tx_inst0|altlvds_tx:ALTLVDS_TX_component|lvds_tx_lvds_tx:auto_generated|arriav_serdes_dpa1' is not properly connected on the 'TXFCLK' port. It must be connected to one of the valid ports listed below.

Info: Can be connected to LVDSCLK port of arriav_pll_lvds_output WYSIWYG
Info: Can be connected to OUTCLK port of generic_pll WYSIWYG

The workaround is to add an LVDS clock buffer between the Altera PLL and the ALTVDS RX and TX instances.

In the links below there are example projects in VHDL and Verilog which shows how these connections are done for an Arria V device.

http://www.altera.com/support/kdb/solutions/rd04102013_389.html

In summary the following connections are needed though the LVDS buffer:

outclk 0 needs to be mapped to the (rx/tx)_inclock port

outclk1 needs to be mapped to the (rx/tx)_enable port

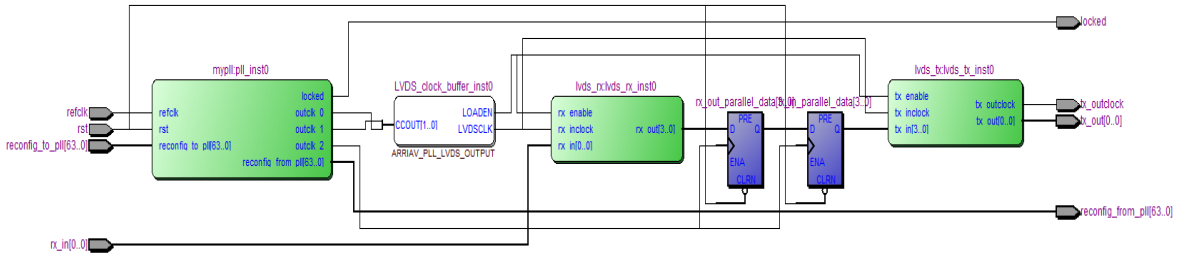

Figure 3-2. LVDS Interface with the Altera_PLL megafunction (Without DPA and Soft-CDR Mode) in Arria V using LVDS buffer workaround

4. Cyclone V Devices

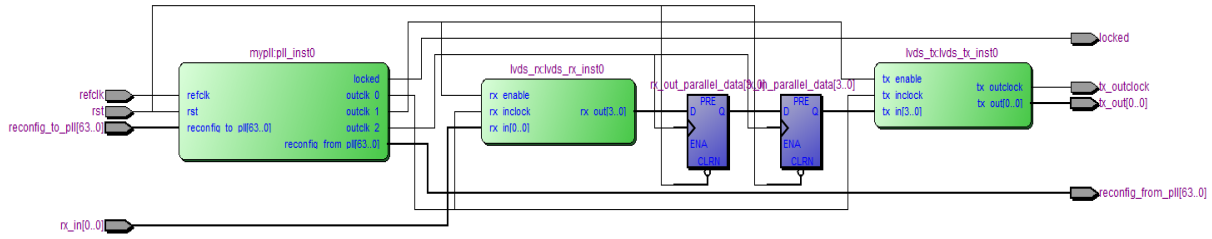

Figure 4-1. LVDS Interface with the Altera_PLL megafunction in Cyclone V devices using LVDS buffer workaround

ERROR messages produced by Mapper for ALTLVDS_RX in external PLL mode

Error: IR FIFO USERDES Block node 'lvds_rx:lvds_rx_inst0|altlvds_rx:ALTLVDS_RX_component|lvds_rx_lvds_rx:auto_generated|sd2' is not properly connected on the 'WRITECLK' port. It must be connected to one of the valid ports listed below.

Info: Can be connected to LOADEN port of arriav_pll_lvds_output WYSIWYG
Info: Can be connected to OUTCLK port of generic_pll WYSIWYG
Info: Can be connected to LVDSCLK port of cyclonev_pll_lvds_output WYSIWYG
Info: Can be connected to OUTCLK port of arriav_clkena WYSIWYG

ERROR messages produced by Mapper for ALTLVDS_TX in external PLL mode

Error: IR FIFO USERDES Block node 'lvds_tx:lvds_tx_inst0|altlvds_tx:ALTLVDS_TX_component|lvds_tx_lvds_tx:auto_generated|lvds_outclk_tx_serialiser' is not properly connected on the 'LOADEN' port. It must be connected to one of the valid ports listed below.

Info: Can be connected to LOADEN port of arriav_pll_lvds_output WYSIWYG
Info: Can be connected to LOADEN port of cyclonev_pll_lvds_output WYSIWYG
Info: Can be connected to OUTCLK port of generic_pll WYSIWYG
Info: Can be connected to OUTCLK port of arriav_clkena WYSIWYG

In the links below there are example projects in VHDL and Verilog which shows how these connections are done for a Cyclone V device.

http://www.altera.com/support/kdb/solutions/rd04102013_389.html

In summary the following connections are needed though the LVDS buffer:

outclk 0 needs to be mapped to the (rx/tx)_inclock port

outclk1 needs to be mapped to the (rx/tx)_enable port

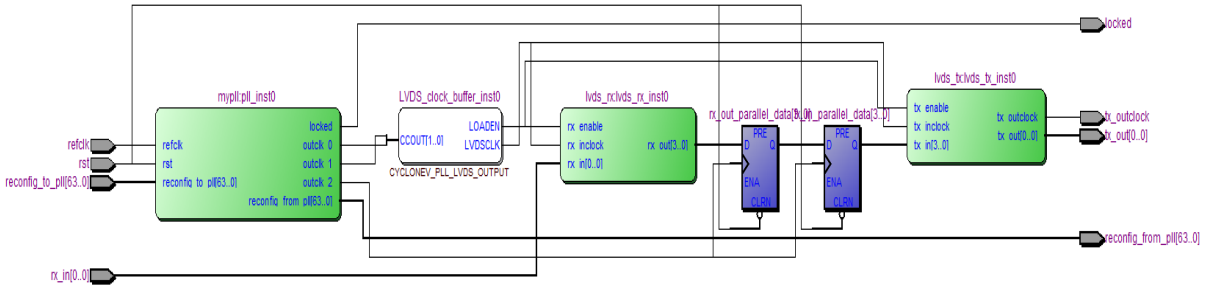

Figure 4-2. LVDS Interface with the Altera_PLL megafunction in Cyclone V devices using LVDS buffer workaround

5. Stratix V Devices

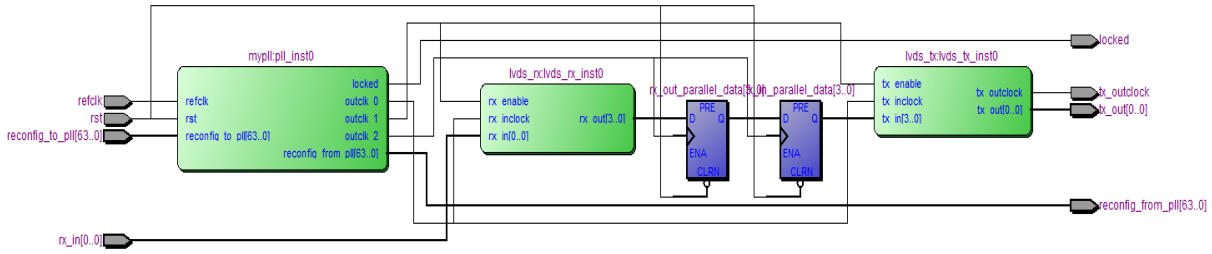

Figure 5-1. LVDS Interface with the Altera_PLL megafunction (Without DPA and Soft-CDR Mode) in Stratix V devices

ERROR messages produced by Mapper for ALTLVDS_RX in external PLL mode

Error: SERDES receiver node 'lvds_rx:lvds_rx_inst0|altlvds_rx:ALTLVDS_RX_component|lvds_rx_lvds_rx:auto_generated|rx_0' is not properly connected on the 'CLOCK0' port. It must be connected to one of the valid ports listed below.

Info: Can be connected to LVDSCLK port of stratixv_pll_lvds_output WYSIWYG
Info: Can be connected to OUTCLK port of generic_pll WYSIWYG

ERROR messages produced by Mapper for ALTLVDS_TX in external PLL mode

Error: SERDES transmitter node 'lvds_tx:lvds_tx_inst0|altlvds_tx:ALTLVDS_TX_component|lvds_tx_lvds_tx:auto_generated|outclock_tx' is not properly connected on the 'ENABLE0' port. It must be connected to one of the valid ports listed below.

Info: Can be connected to LOADEN port of stratixv_pll_lvds_output WYSIWYG
Info: Can be connected to OUTCLK port of generic_pll WYSIWYG

In the links below there are example projects in VHDL and Verilog which shows how these connections are done for a Stratix V device.

http://www.altera.com/support/kdb/solutions/rd04102013_389.html

In summary the following connections are needed though the LVDS buffer:

outclk 0 needs to be mapped to the (rx/tx)_inclock port

outclk1 needs to be mapped to the (rx/tx)_enable port

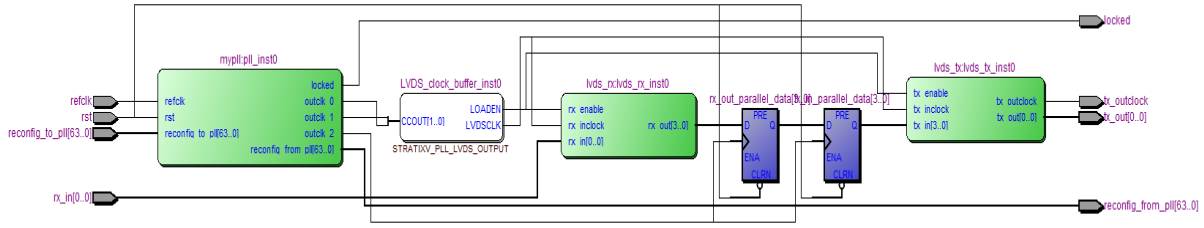

Figure 5-2. LVDS Interface with the Altera_PLL megafunction (Without DPA and Soft-CDR Mode) in Stratix V devices using LVDS buffer workaround

6. Conclusion

This document demonstrated how to add an LVDS buffer in your RTL when using dynamic phase stepping or PLL reconfiguration on the Altera_PLL when interfacing to the ALTLVDS_RX and ALTLVDS_TX megafunctions using external PLL mode. The LVDS buffer is required to avoid analysis and synthesis errors in the Quartus II software when using ALTLVDS in external PLL mode.

7. Revision History

Revision	Changes Made	Date
V1.0	Initial release.	April 2013