Altera Nios II Release Notes

2016.06.17

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These release notes cover versions 15.1 through 16.0 of the Altera® Nios® II Embedded Design Suite (EDS) software and Nios II processor IP core.

For the most recent list of errata for the Nios II EDS, search the Knowledge Base on the Altera website. You can use the Knowledge Base to search for errata based on the product version affected and other criteria.

Note: This document is the first release of the combined *Nios II IP Core Release Notes* and *Nios II Embedded Design Suite Release Notes*. To access past versions of the release notes, search the "Altera Documentation Archive" web page.

Related Information

- **Nios II Release Notes (Archived)**
- **Altera Knowledge Base**
  For more information about errata and other potential issues, enter a keyword in the search field.

Nios II 16.0 Release Notes

Nios II Processor IP 16.0 Release Notes

The floating-point hardware 2 (FPH2) IP has been enhanced to support the ability to include or exclude groups of custom instructions, such as arithmetic, conversions, and comparisons, so that you can omit groups of instructions that are not needed and save logic resources. Support for each selected custom instruction is automatically extended into the software when the board support package (BSP) is generated.

Nios II EDS 16.0 Release Notes

- The GNU Compiler Collection (GCC) for the Nios II processor has been upgraded to version 5.2.

  Note: For more information about what is in the 5.2 version, refer to the *GCC, the GNU Compiler Collection* website.

Embedded IP 16.0 Release Notes

- New IP core added to Qsys:
  - Altera I²C Slave to Avalon® Master Bridge IP.
- Feature enhancements to MAX® 10 FPGA analog-to-digital converter (ADC) interface IP:
  - Support for variable ADC sampling frequencies (1 MHz to 25 KHz).
  - The ADC simulator is able to read voltages from a text file and output a correct converted value.
- Maximum buffer size for the 16550 UART IP has been increased up to 256 words.

Related Information

- **GCC, the GNU Compiler Collection website**
  For more information about the GCC releases, refer to the *GCC, the GNU Compiler Collection* website.
- **Nios II Processor and EDS New Features**
  For the latest information about what is new in your version of Nios II, refer to the Nios II web pages and the "What's New" section of the Nios II pages on the Altera website.

Nios II 15.1 Release Notes

Nios II Processor IP 15.1 Release Notes

- The floating-point hardware 2 (FPH2) IP has been enhanced to support optional exclusion of the `sqrt()` custom instruction. (1) In some MAX 10 device configuration modes, FPGA memory block initialization is not supported, which means that this instruction does not function correctly with those configuration modes. In these cases, the instruction can be manually omitted from the FPH2 module allowing the `sqrt()` operation to execute correctly in the software implementation of the instruction.
- In Qsys, the Nios II Gen2 processor is called the "Nios II Processor".

  Note: The register transfer level (RTL) name remains the same.
- The Qsys graphical user interface (GUI) for the Nios II vectored interrupt controller (VIC) has been modified; a widget has been added that allows selection of the number of pipeline stages used in the core. The default value is five cycles latency but with the new GUI option this can be reduced, although the penalty for this is a reduction in the f_{MAX} of the VIC.

Nios II EDS 15.1 Release Notes

- The GNU Compiler Collection (GCC) for the Nios II processor has been upgraded to version 4.9.2.

  Note: For more information about what is in the 4.9.2 version, refer to the *GCC, the GNU Compiler Collection* website.
- New MAX 10 ADC Hardware Abstraction Layer (HAL) driver.
- New Quad Serial Peripheral Interface (QSPI) HAL driver.
- Enhancements to the MAX 10 ADC HAL driver.

(1) The `sqrt()` instruction is a look-up table based implementation and relies on a pre-populated FPGA memory.

GCC for Nios II v4.9.2 Release Notes

- Code density and performance—Use of the `-mgpopt=global` setting is recommended as it generally delivers results with better code density and performance.[2]
- C++ code size reduction: `-fno-exceptions`—When you are using C++ but trying not to link in the (big) C++ exception-handling machinery `nios2-elf-g++` will, in some cases, link in the exception-handling machinery where it is not actually required. This switch suppresses that behaviour, which results in a smaller code footprint for those situations.
- Response to address 0x00 access: `-fdelete-null-pointer-checks`—You often have RAM at address 0x00 (== NULL pointer in gcc and most C compilers). From gcc 4.9 onwards, by default gcc detects attempts to read or write to address 0x00 and converts them to traps; typically in embedded/Nios II-based systems, these traps are not handled so the code will fail silently. This means that code that works when compiled with earlier versions of gcc could silently fail when compiled with gcc-4.9 (onwards).

  Note: In order to avoid this for Nios II, this behaviour has been modified so that accesses to address 0x00 will work as expected for Nios II systems but there may be a slight negative effect on code performance. In Nios II systems that are known not to read or write RAM at address 0x00, use of the switch `--fdelete-null-pointer-checks` restores the original gcc behaviour and may provide a small performance boost.
- Expansion of `__builtin_trap`—As of v15.1, GCC produces trap 3 instead of break 3 in the expansion of the `__builtin_trap` function and in other situations where a trap is emitted to indicate undefined runtime behaviour. [3]
- Memory corruption bug fix—The long pathnames on Windows hosts that could lead to memory corruption, causing potential crashes and unpredictable behaviour, has been fixed.
- GDB breakpoint instruction—As of v15.1, GDB uniformly uses trap 31 instead of a break instruction for software breakpoints. [4]

Embedded IP 15.1 Release Notes

- A descriptor prefetcher option has been added to the modular Scatter-Gather Direct Memory Access (mSGDMA) IP core to automatically fetch descriptors from memory.
- Optional support for 9-bit data and the sticky bit has been added to the 16550 UART IP.

Related Information

- **GCC, the GNU Compiler Collection website**
  For more information about the GCC releases, refer to the *GCC, the GNU Compiler Collection* website.
- **Nios II Processor and EDS New Features**
  For the latest information about what is new in your version of Nios II, refer to the Nios II web pages and the "What's New" section of the Nios II pages on the Altera website.

[2] This requires that everything is compiled with the same `-Gn` switch setting; use of `-Gn` is not generally recommended.
[3] This is for compliance with the Nios II ABI for Linux targets, which does not permit the use of the break instruction in user code.
[4] This is for consistency with the Nios II ABI for Linux targets.

Document Revision History for the Nios II Processor

Date	Version	Changes
June 2016	2016.06.17	Initial release of the combined Nios II release notes.