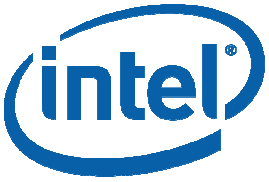

Intel® C600 Series Chipset

Boundary Scan Testability

February 2012

Document Number: 326516-001

Contents

1 Introduction 5

1.1 About this Document 5

2 Intel® C600 Series Chipset BSDL Overview 7

2.1 One BSDL for all SKUs 7

3 Intel® C600 Series Chipset JTAG/Boundary Scan Test Mode 10

3.1 TAP Controller 10
3.2 JTAG Test Entry Mode 11
3.3 JTAG Instructions 13
3.4 JTAG Data Registers 14
3.4.1 Boundary Data Register 14
3.4.2 Bypass Data Register 14
3.4.3 IDCODE Data Register 14

Figures

Figure 3-1. TAP Controller 10
Figure 3-2. Boundary Scan Test Mode Entry 12

Tables

Table 3-1 TAP Signal Definitions 11
Table 3-2. JTAG Instruction Register Description 13

Revision History

Document Number	Revision Number	Description	Date
326516	-001	• Initial release of the document.	Feb 2012

1 Introduction

1.1 About this Document

This document will be used as a support document for Intel® C600 Series Chipset BSDL.

This document is intended for the development of IEEE 1149.6 Boundary scan tests for Intel® C600 Series chipset products. This manual assumes a working knowledge of IEEE 1149.6 methodologies and the in circuit test(ICT) manufacturing test methods.

Chapter 1. Introduction
Chapter 1 provides information on the organization of this Document.

Chapter 2. Intel® C600 Series Chipset BSDL Overview
Chapter 2 provides a detailed discussion of the Intel® C600 Series Boundary Scan dependence on the different SKUs and testing scenarios.

Chapter 3. JTAG boundary Scan Test Mode
Chapter 3 provides an overview of TAP controller, how to use the TAP to power up the system to use boundary scan. Also explains the different instructions in the scan.

Note: This document applies to all Intel® C600 Series Chipset SKUs.

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2 Intel® C600 Series Chipset BSDL Overview

This section will assist in managing the Intel® C600 Series chipset BSDL file to generate boundary scan tests that are based on product design and the Intel® C600 Series chipset purchase SKU. There are currently five SKU's supported which are C602(-A), C602J(-J), C604(-B), C606(-D) and C608(-T).

2.1 One BSDL for all SKUs

The Intel® C600 Series chipset product family has four different SKUs and only one BSDL file that will be used with all SKUs. All of the Intel® C600 Series chipset SKUs will have the same boundary scan chain length. Based on the purchased SKU of the Intel® C600 Series chipset and the status of the VCCXUS power pins, the PEG0_RX and PEG0_TX signals will not be powered.

For Intel® C600 Series chipset the following table lists out the changes required base on SKU and VCCXUS power status.

SKUs	VccXUS Status	BSDL Modification Required	Cell Numbers To Be Modified	Modified Cell Type
C602(-A), C606(-D), C608(-T)	Vcc	No	N/A	N/A
C602(-A), C606(-D), C608(-T)	Vss	Yes	205-207, 209-211, 213-215, 217-219	Internal
C604(-B)	N/A	Yes	205-207, 209-211, 213-215, 217-219	Internal
C602J(-J)	N/A	Yes	205-207, 209-211, 213-215, 217-219	Internal

2.2 Individual line updates in BSDL file

If there is a requirement to change BSDL, simply follow the below suggested changes. Replace the "Change From" section with "Change To" section and comment out any sections listed below.

```
-- Change From:
```

```
" 205( bc_4     , PEG0_RP_3            , input            , X ),"  &
" 206( bc_4     , PEG0_RN_3            , input            , X ),"  &
" 207( ac_1     , PEG0_TP_3            , output2          , X ),"  &

" 209( bc_4     , PEG0_RP_2            , input            , X ),"  &
" 210( bc_4     , PEG0_RN_2            , input            , X ),"  &
" 211( ac_1     , PEG0_TP_2            , output2          , X ),"  &

" 213( bc_4     , PEG0_RP_1            , input            , X ),"  &
" 214( bc_4     , PEG0_RN_1            , input            , X ),"  &
" 215( ac_1     , PEG0_TP_1            , output2          , X ),"  &

" 217( bc_4     , PEG0_RP_0            , input            , X ),"  &
" 218( bc_4     , PEG0_RN_0            , input            , X ),"  &
" 219( ac_1     , PEG0_TP_0            , output2          , X ),"  &


-- Change To:

" 205( bc_1     , *                    , internal         , X ),"  &
" 206( bc_1     , *                    , internal         , X ),"  &
" 207( bc_1     , *                    , internal         , X ),"  &

" 209( bc_1     , *                    , internal         , X ),"  &
" 210( bc_1     , *                    , internal         , X ),"  &
" 211( bc_1     , *                    , internal         , X ),"  &

" 213( bc_1     , *                    , internal         , X ),"  &
" 214( bc_1     , *                    , internal         , X ),"  &
" 215( bc_1     , *                    , internal         , X ),"  &

" 217( bc_1     , *                    , internal         , X ),"  &
" 218( bc_1     , *                    , internal         , X ),"  &
" 219( bc_1     , *                    , internal         , X ),"  &


-- The following should be commented out:

-- --"Differential_Voltage ((PEG0_TP_3,PEG0_TN_3)),"&
-- --"Differential_Voltage ((PEG0_TP_2,PEG0_TN_2)),"&
-- --"Differential_Voltage ((PEG0_TP_1,PEG0_TN_1)),"&
-- --"Differential_Voltage ((PEG0_TP_0,PEG0_TN_0)),"&

-- --"PEG0_RP_3             [205] :                HP_time=8.0e-9 ; " &
-- --"PEG0_RN_3             [206] :                HP_time=8.0e-9 ; " &
-- --"PEG0_TP_3                                    ; " &
-- --"PEG0_RP_2             [209] :                HP_time=8.0e-9 ; " &
-- --"PEG0_RN_2             [210] :                HP_time=8.0e-9 ; " &
-- --"PEG0_TP_2                                    ; " &
-- --"PEG0_RP_1             [213] :                HP_time=8.0e-9 ; " &
-- --"PEG0_RN_1             [214] :                HP_time=8.0e-9 ; " &
-- --"PEG0_TP_1                                    ; " &
-- --"PEG0_RP_0             [217] :                HP_time=8.0e-9 ; " &
-- --"PEG0_RN_0             [218] :                HP_time=8.0e-9 ; " &
-- --"PEG0_TP_0                                    ; " &
```

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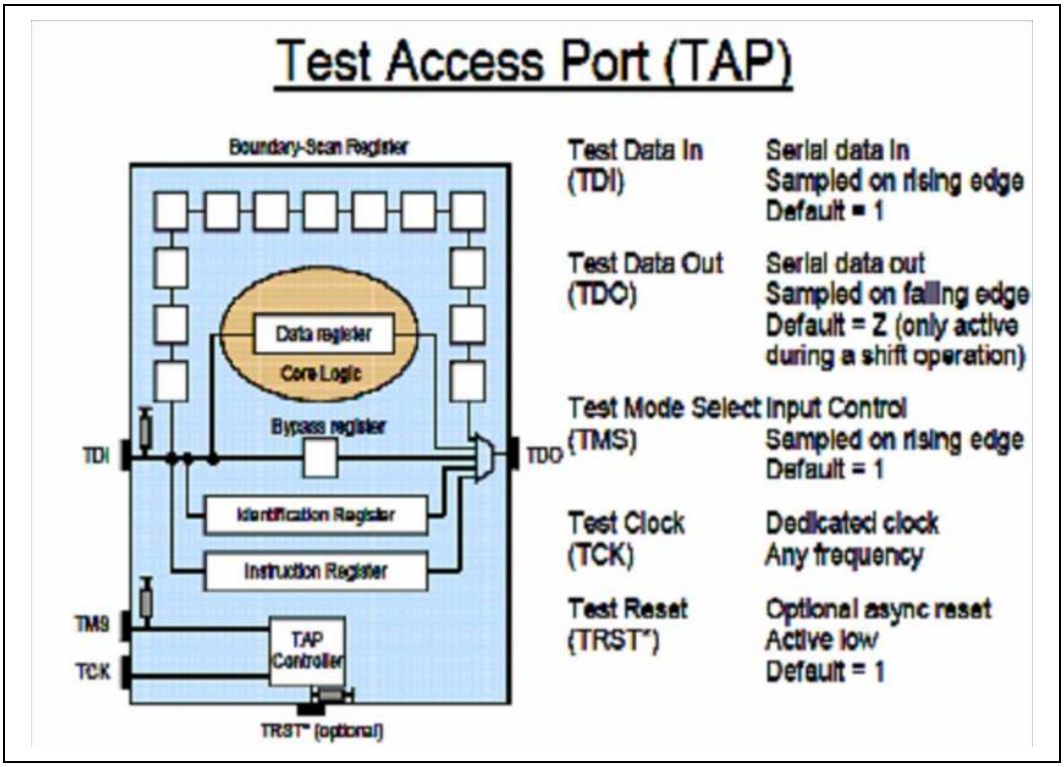
3 Intel® C600 Series Chipset JTAG/Boundary Scan Test Mode

3.1 TAP Controller

The Intel® C600 Series chipset has dedicated JTAG pins and TAP controller as shown in Figure 3-1. For detailed information on functionality of the interface, please refer to specifications *IEEE Standard Test Access Port and Boundary Scan Architecture 1149.1-2001 Specification* and *1149.6- IEEE Standard for Boundary-Scan Testing of Advanced Digital Networks – Specification*.

Figure 3-1. TAP Controller



In order to support boundary scan for AC coupled, high-speed IOs the master TAP supports IEEE 1149.6. This includes the extra instructions extest_pulse and extest_train. There is also an additional instruction that is not in the IEEE 1149.6 spec, defined by Intel - extest_toggle. For details on supported Boundary Scan Instructions refer to Table 3-2. The Intel® C600 Series TAP network is accessed serially through four dedicated component pins as shown in Table 3-1.

Note: The 1149.1 specification also defines an optional TRST# TAP input pin, to asynchronously reset the TAP controllers. However, the Intel® C600 Series chipset does not implement this pin. Instead each TAP controller is asynchronously reset by an internal power OK signal corresponding to the power well that it is in.

Table 3-1 TAP Signal Definitions

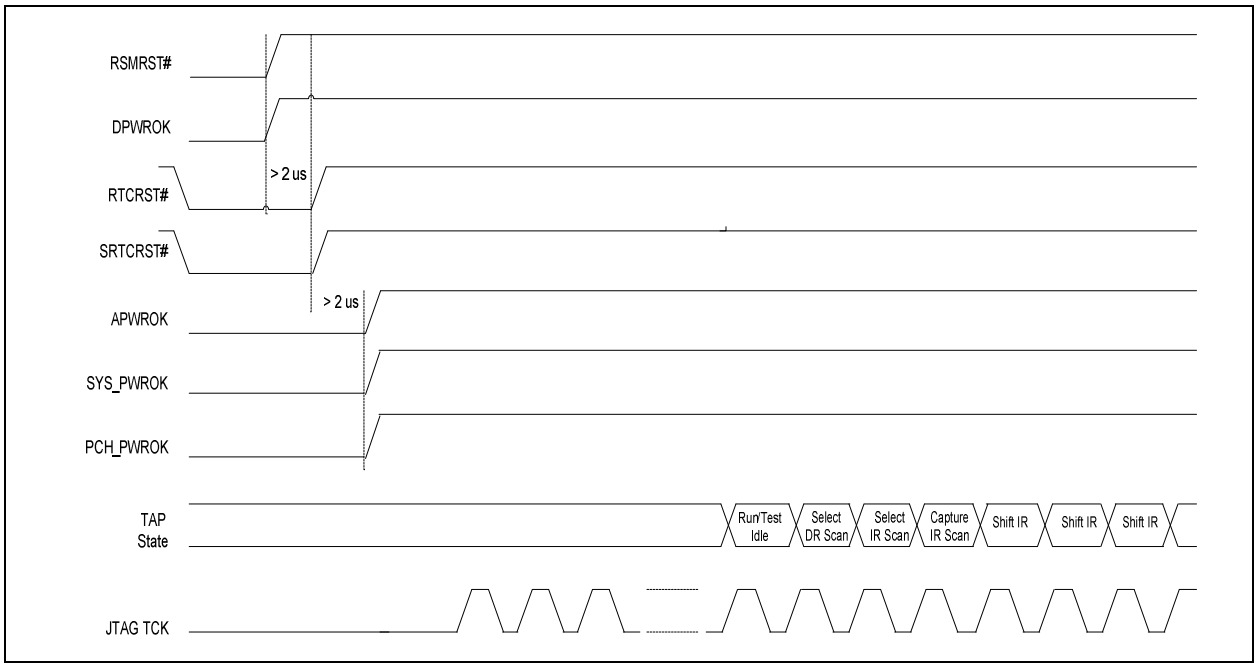
Name	Description
TCK	TAP Clock input
TMS	Test Mode Select. Controls the TAP finite state machine
TDI	Test Data Input. The serial input for test data
TDO	Test Data Output. The serial output for the test data

During Boundary Scan Test mode, boundary scan unit will take over the IO/AFE control for direct control to execute all the different IEEE 1149.1 and 1149.6 instructions.

3.2 JTAG Test Entry Mode

In order to enter the Boundary Scan test mode multiple signals must be conditioned correctly. The test mode entry sequence is outlined in Figure 3-2 and the text that follows. The test entry sequence is targeted towards ICT that are invasive bed-of-nail testers that can prohibit a board from sequentially powering up and maintaining running on board clocks. The test entry sequence is not needed for board designs that can power up in an orderly fashion.

Figure 3-2. Boundary Scan Test Mode Entry



Signal Details:

- RSMRST# is a hard reset to indicate the SUS well is valid
- DPWROK is a hard reset to indicate the DSW well is valid
- RTCRST# is a hard reset to indicate the RTC well is valid
- SRTCRST# is a hard strap for reset and isolation override
- APWROK is a hard reset to indicate the ME well is valid
- PCH_PWROK is a hard reset to indicate the CORE well is valid
- SYS_PWROK is hard reset to indicate the system has been powered up
- INTVRMEN and DSWOVRMEN are the non reset pins incorporated with power up signals.
- INTVRMEN and DSWOVRMEN connect to Vss to disable VRM and connect to VccRTC power plane to enable VRM.
- INTVRMEN and DSWOVRMEN should be set to Vss or VccRTC, based on the board design throughout the entire boundary scan test

Power Up sequence:

- RSMRST# needs to be driven from 0-> 1
- DPWROK needs to be driven from 0-> 1 (can be driven same time or DPWROK can be driven to 1 after RSMRST# is driven to 1.

— Followed by RTCRST# driven from 0->1 (~2us later or more). Can be driven at the same time with SRTCRST# when connected together.
  - Followed by APWROK driven from 0-> 1 (~2us later or more)
  - Followed by SYS_PWROK driven from 0->1 (~2us later or more)
  - Followed by PCH_PWROK driven from 0-> 1 (~2 us later or more)

Test Mode Entry details:

- SRTCRST# is a reset and isolation override hard strap. This hard strap enables boundary scan when driven to '0' when DPWROK is '1'. Needed primarily if on board clocks are not running. SRTCRST# can be released after RTCRST# transition from 0->1 if not connected to RTCRST#. SRTCRST# is latched on the rising edge of DPWROK#.

Supported TCK frequencies:

- The supported maximum frequency of TCK will be 2MHz. A delay will be observed on the response of TDO with regard to the falling edge of TCK.

3.3 JTAG Instructions

JTAG instruction register commands related to boundary scan as in Table 3-2 are implemented in the Intel® C600 Series chipset.

Table 3-2. JTAG Instruction Register Description

Bit[7:0]	Instruction	Description
00h	**EXTEST**	Selects the Boundary data register that controls the I/O for board level connectivity testing.
01h	**SAMPLE**	Selects the Boundary data register and allows a snapshot to be taken of the states of the component's input and output signals without interfering with the normal operation of the assembled board.
02h	**PRELOAD**	Selects the Boundary data register and allows data values to be loaded onto the latched parallel outputs of the boundary-scan shift register before selection of the other boundary-scan test instructions.
03h	**HIGHZ**	Selects the Bypass data register and places the component in a state in which *all* of its system logic outputs are placed in an inactive drive state (e.g., high impedance).
04h	**CLAMP**	Allows the state of the signals driven from component pins to be determined from the boundary-scan register while the Bypass data register is selected as the serial path between TDI and TDO.
05h	**IDCODE**	Reads a 32 bit register that contains the Manufacturers Identity, Part Number and Version.

Bit[7:0]	Instruction	Description
06h	**EXTEST_TOGGLE**[1]	An Intel specific instruction that will toggle the output pins at ½ the frequency of the TCK, if the value in Boundary Scan cell is '1', and drive constant '0' if the value in Boundary Scan cell is '0'.
07h	**EXTEST_TRAIN**	An 1149.6 instruction for AC signals that selects the Boundary data register and toggles the output pins. Non 1149.6 pin behave like EXTEST command.
08h	**EXTEST_PULSE**	An 1149.6 instruction for AC signals that selects the Boundary data register and generates a pulse at the output pins. Non 1149.6 pin behave like EXTEST command.
FFh	**BYPASS**	Selects the Bypass data register that contains a single shift-register stage and is used to provide a minimum-length serial path between the TDI and the TDO pins of a component when no test operation of that component is required.

NOTES:

1. EXTEST_TOGGLE is implemented in many of the cells. Refer to the BSDL for the pins that support the EXTEST_TOGGLE instruction.

3.4 JTAG Data Registers

The following describes the data registers that are used.

3.4.1 Boundary Data Register

Bit	Reset	Description
479: 0	X	480 bit register

3.4.2 Bypass Data Register

Bit	Reset	Description
1	0	1 bit register

3.4.3 IDCODE Data Register

Bit	Reset	Description
31:28	BSDL[1]	**Version:** Used to identify variant of component type.
27:12	A110h	**Part number:** Unique value to represent the component.

11:1	00000 00100 1b	**Manufacturer Identity:** Intel identity is 00000001001b
0	1b	**Hardcode to '1'** as indication of start of IDCODE.

NOTES:

1. Refer to the BSDL file for the version used.

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